FINE-PITCH CU-SNAG DIE-TO-DIE AND DIE-TO-INTERPOSER INTERCONNECTIONS USING ADVANCED SLID BONDING

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FINE-PITCH CU-SNAG DIE-TO-DIE AND DIE-TO-INTERPOSER INTERCONNECTIONS USING ADVANCED SLID BONDING

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SUMMARY

Multi-chip integration with emerging technologies such as a 3D IC stack or 2.5D interposer is primarily enabled by the off-chip interconnections. The I/O density, speed and bandwidth requirements for emerging mobile and high-performance systems are projected to drive the interconnection pitch to less than 20 microns by 2015. A new class of low-temperature, low-pressure, high-throughput, cost-effective and maufacturable technologies are needed to enable such fine-pitch interconnections.

A range of interconnection technologies are being pursued to achieve these fine-pitch interconnections, most notably direct Cu-Cu interconnections and copper pillars with solder caps. Direct Cu-Cu bonding has been a target in the semiconductor industry due to the high electrical and thermal conductivity of copper, its high current-carrying capability and compatibility with CMOS BEOL processes. However, stringent coplanarity requirements and high temperature and high pressure bonding needed for assembly have been the major barriers for this technology.

Copper-solder interconnection technology has therefore become the main workhouse for off-chip interconnections, and has recently been demonstrated at pitches as low as 40 microns. However, the current interconnection approaches using copper-solder structures are not scalable to finer feature sizes due to electromigration, and reliability issues arising with decreased solder content. Solid Liquid Inter-Diffusion (SLID) bonding is a promising solution to achieve ultra-fine-pitch and ultra-short interconnections with a copper-solder system, as it relies on the conversion of the entire solder volume into thermally-stable and highly electromigration-resistant intermetallics with no residual solder. Such a complete conversion of solders to stable intermetallics, however, relies on a long assembly time or a subsequent post-annealing process.

To achieve pitches lower than 30 micron pitch, this research aims to study two ultra-short copper-solder interconnection approaches: (i) copper pillar and solder cap technology, and (ii) a novel technology which will enable interconnections with improved electrical performance by fast and complete conversion of solders to stable intermetallics (IMCs) using Solid Liquid Diffusion (SLID) bonding approach. SLID bonding, being a liquid state diffusion process, combined with a novel, alternate layered copper-solder bump structure, leads to higher diffusion rates and a much faster conversion of solder to IMCs. Moreover this assembly bonding is done at a much lower temperature and pressure as compared to that used for Cu-Cu interconnections.

FEM was used to study the effect of various assembly and bump-design characteristics on the post-assembly stress distribution in the ultra-short copper-solder joints, and design guidelines were evolved based on these results. Test vehicles, based on these guidelines, were designed and fabricated at 50 and 100 micron pitch for experimental analysis. The bumping process was optimized, and the effect of current density on the solder composition, bump-height non-uniformity and surface morphology of the deposited solder were studied. Ultra-short interconnections formed using the copper pillar and solder cap technology were characterized.

A novel multi-layered copper-solder stack was designed based on diffusion modeling to optimize the bump stack configuration for high-throughput conversion to stable Cu_3Sn intermetallic. Following this modeling, a novel bumping process with alternating copper and tin plating layers to predesigned thicknesses was then developed to fabricate the interconnection structure. Alternate layers of copper and tin were electroplated on a blanket wafer, as a first demonstration of this stack-technology. Dies with copper-solder test structures were bonded using SLID bonding to validate the formation of stable intermetallics.

CHAPTER 1

INTRODUCTION

Electronic systems have become an essential part of our daily lives. They enable us to compute, communicate, entertain and make life more convenient. Small devices, which can fit in our pockets, have become powerful enough to connect people on the other side of the globe. All this has been made possible by the dramatic growth in the microelectronics industry. The two major driving factors for this growth have hitherto been (i) the invention of the integrated circuit in 1958 [1], and (ii) transistor scaling.

1.1 Transistor Scaling and Moore's Law

Transistor scaling has not only led to many technology advances in the semiconductor industry, but has also resulted in a rapid miniaturization of devices. Based on his observations on transistor scaling adopted in the industry, Gordon Moore formulated the Moore's law in 1965 [2], which predicted the doubling of the number of transistors on integrated circuits every two years. Although Moore's Law was initially an observation, industry soon started using this as a goal.

The industry has kept pace with Moore's Law for over 40 years. Major advances in lithography have enabled the 22nm technology node, which is currently in high volume production [3]. Further, the 14nm technology has already been demonstrated and 10nm and 7nm technologies are under development [4]. As the semiconductor industry moves towards production of chips with 14nm nodes, the transistor count on these chips will be over a billion, the I/O requirements will be over 10,000, and power levels more than 150 watts. The need for such high I/O densities, combined with lower power, will drive the off-chip interconnection pitches to less than 20 microns by 2015 as indicated in Figure 1 (David McCann, Global Foundries).

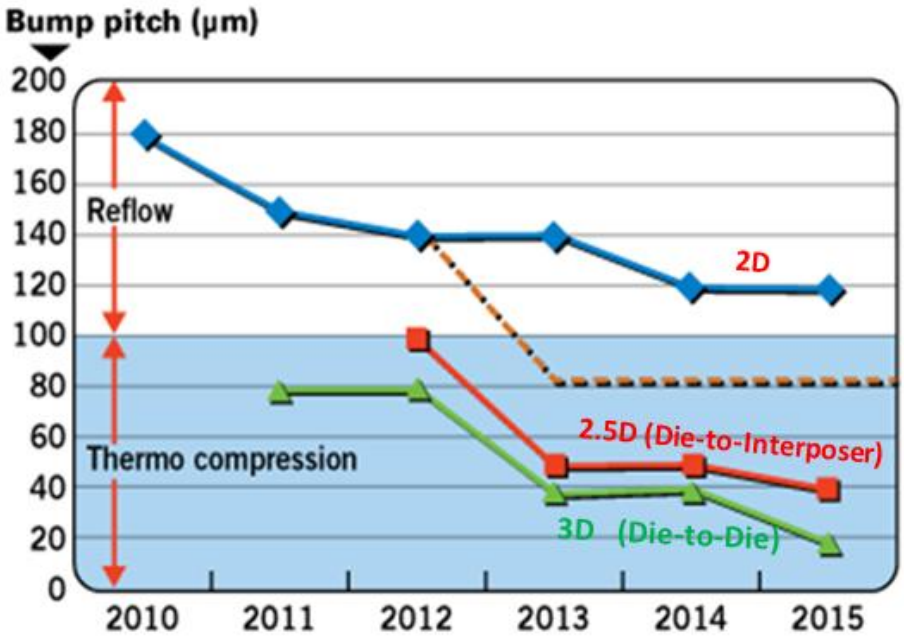


Figure 1: Short-term roadmap for off-chip interconnection pitch (Courtesy: David McCann)

Figure 1 shows the global roadmap for off-chip interconnection pitch for a number of packaged devices in 2D, 2.5D (die-to-interposer) and 3D (die-to-die), showing the need for off-chip interconnections below 20 microns by 2015. This trend is expected to continue beyond 2015.

1.2 Trends for Next-Generation Off-chip Interconnections

The interconnections have continuously evolved from peripheral wire-bonding technologies to area-array flip-chip interconnections to meet the need for higher I/Os and enhanced electrical performance. Although wire-bonding has been scaled down to finer pitch of less than 60 microns, they are now relegated to low-performance ICs with low I/O counts**.** High performance devices requiring higher I/Os and higher performance are primarily enabled by flip-chip interconnection technology. In this technology, the chip is placed with its active side facing down and bonded to the substrate using an array

of solder joints. The key benefits of this technology are: (i) incorporation of I/Os across the whole chip area, thus increasing the number of I/Os, (ii) reduction of the interconnection height to improve the electrical performance with lower parasitic inductance, capacitance and resistance, (iii) ability to cool the IC from the back of the IC for more effective thermal management, and (iv) design flexibility.

The invention of underfill, the advances in low CTE substrates and the development of polymer-copper thin-film wiring layers leading to fine pitch bumps have led flip-chip technologies address the I/O pitch scaling from 225 microns in 1980s to less than 100 microns today. Various flip-chip interconnection materials and processes have been developed over the past two decades. These include lead-free solders, gold stud bumps, copper-solder and copper-copper interconnections. Gold stud bumping has several shortcomings such as the cost and bump-non-coplanarity across the die, and is only used for certain niche applications. Lead-free solder bumps have been serving the industry for the past 10 years, but face shortcomings for emerging fine-pitch applications because of issues such as solder bridging and electromigration.

The invention of copper pillar technology has successfully addressed the limitations of lead-free solders, leading to I/O pitch below 60 microns. In this approach, the interconnection bump structure consists of solder deposited on top of a tall copper pillar. The copper pillar provides several advantages such as: finer pitch capability by prevention of solder bridging, suppression of electromigration, and enhancement in thermo-mechanical reliability from higher stand-off height.

Direct copper-copper interconnections without solders have the highest current-handling and lowest pitch capabilities. However, there are fundamental challenges associated with these that include a high temperature solid-state bonding process, inability to accommodate non-planarity and non-uniformity of interconnection bumps, and complex processes that are required for the removal of residual oxides on the copper

surfaces prior to bonding. GT-PRC has made pioneering advances in direct Cu-Cu interconnections at low temperature using liquid-enhanced bonding to obtain copper interconnections without solder. This technology is in the early stages of development and is not in manufacturing. Due to the above challenges associated with copper interconnections, copper-solder interconnection is still the preferred approach in the semiconductor industry.

1.3 Challenges with Next Generation of Solder-based Interconnection Technologies

Three major challenges need to be addressed for solder-based technologies to be scaled down to lower feature sizes. The first challenge comes from reliability issues faced during assembly due to low solder volume in ultra-thin interconnections. There is a considerable difference in the mechanical properties of the IMCs and the residual solder in the bump, leading to stresses developing at the IMC-solder interface. With the trend towards interconnections with lower stand-off height, the resultant small volume of solder is not able to accommodate these stresses. As interconnections approach small feature sizes, processing constraints from solder-bridging become critical. The third challenge faced by fine-pitch solder-based interconnections is that of electromigration [5]. Interconnection size reduces with finer pitch and smaller heights, but the current per interconnection bump remains the same, leading to increased current densities. A decrease in bump diameter from 200 microns to 50 microns leads to a 16 times increase in the current density, as shown in Figure 2 [6]. As a result, the current density in interconnections with pitch of 50 microns and finer is reaching its capacity in terms of current handling.

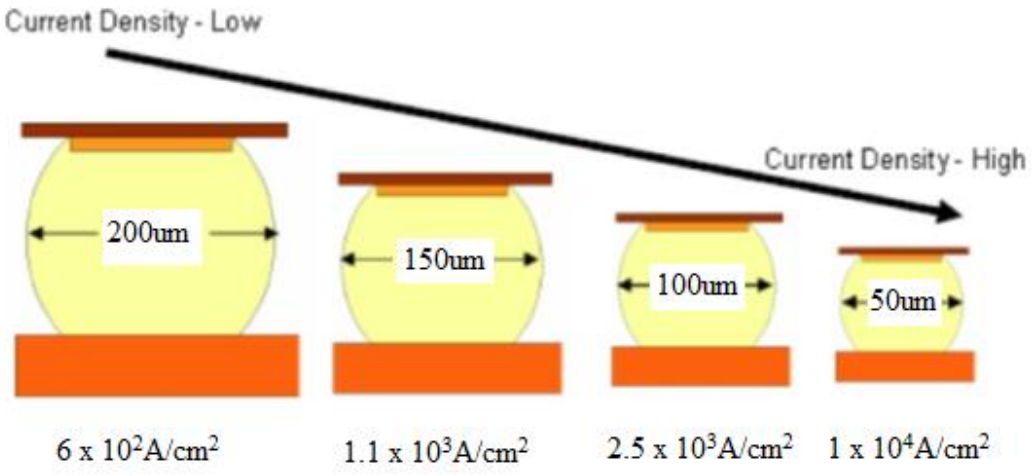


Figure 2: Effect of bump size on current density for a current per bump of 0.2A

1.4 Ultra-Fine-Pitch Copper-Solder Stacked Interconnections

A novel approach, based on a combination of Solid Liquid Inter-Diffusion (SLID) bonding and alternate stacking of copper-solder layers, for faster conversion of copper-solder to thermally-stable and electromigration-resistant intermetallics is proposed. This approach enables assembly with high throughput and yield even at low stand-off heights because of the distributed solder layers that provide controlled collapse without the bridging of solder bumps. This new scheme of interconnections will also address the thermo-mechanical and electromigration reliability concerns from residual solders, associated with fine-pitch solders. This approach also reduces the bonding pressures and temperatures required for high-volume manufacturing compared to Cu-Cu interconnections. Figure 3 schematically shows the proposed interconnection approach as compared to the current approach.

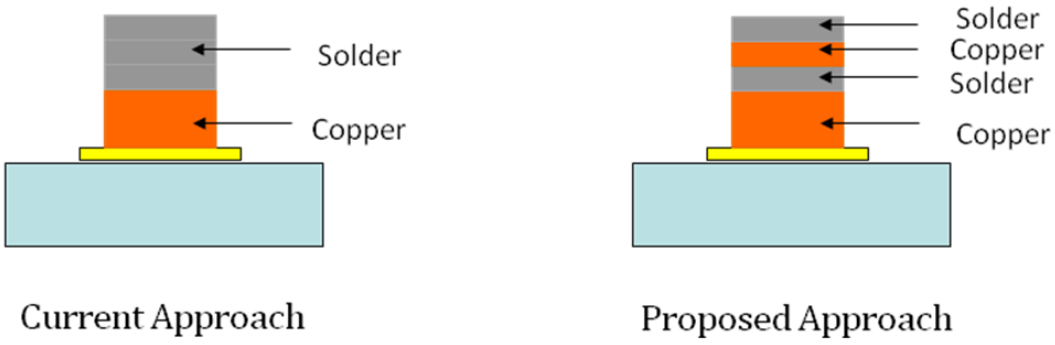


Figure 3: Current and proposed approaches for copper-solder interconnections

Copper and tin form two intermetallics, Cu_6Sn_5 and Cu_3Sn, the latter being the stable intermetallic. The residual solder after assembly reflow in traditional copper-solder interconnections is susceptible to electromigration and thermal-migration. Cu_3Sn, on the other hand, has been shown to have a higher electromigration resistance and better stability as compared to solder [7]. Formation of the stable Cu-Cu_3Sn is the key for the new copper-solder interconnections approach proposed for fine-pitch. In the proposed approach, multiple thin layers of copper and solder are alternately deposited to form the interconnection bump structure. The novelty of the proposed approach provides lower diffusion distances as a result of these alternate thin layers, leading to much faster formation and growth of intermetallics. Thus, the copper-solder can be completely converted to the stable IMC, Cu_3Sn, at a lower temperature and bonding time, as compared to that required in the current approach.

This thesis also investigates the material and processing challenges with ultra-short (<15 micron) copper-solder interconnections on ultrathin glass packages through thermo-mechanical modeling, interconnection design, assembly process and joint characterization.

1.5 Research Objectives and Thesis Organization

The key objective of this research is to demonstrate materials and processes to form fine-pitch off-chip interconnections that are reliable and can handle high current densities. The proposed interconnection bump pitch is 30 microns, with a bump diameter of 15 microns and a stand-off height of 15 microns. The key tasks are to (i) conduct finite-element analysis to investigate the optimum design guidelines for fine-pitch and ultra-thin interconnections with traditional copper-solder approach, (ii) explore bumping and assembly processes, and characterize interconnections fabricated using these design guidelines, (ii) explore and demonstrate a novel interconnection technology using a multi-layer stack of copper-solder to improve the electrical performance by complete conversion of copper and solder to the stable IMC.

This thesis is organized into six chapters. Chapter 1 reviews the previously-reported research in flip-chip and SLID bonding, and presents an innovative idea to advance SLID bonding. Chapter 2 reviews the state-of-the-art interconnection technologies in more detail. Drawbacks of the current interconnection technologies and the need for a new copper-solder-based technology at fine pitches are presented.

Chapter 3 presents results of finite element analysis to determine design guidelines for fine-pitch copper-solder interconnections with low stand-off height. Diffusion modeling is used to design copper-solder interconnections, using a novel approach where the entire solder volume is converted into stable Cu_3Sn intermetallic, using alternate stacked layers of copper and solder.

Chapter 4 focuses on the materials and processes used in this research. The test vehicle design and fabrication process are described. The assembly process and characterization for the die-substrate interconnections is also described.

Chapter 5 presents the results based on the experimental procedures described in the previous chapter. Bumping process development for fine-pitch copper-solder

interconnections is initially presented. This is followed by the characterization of these interconnections, and a study on the effect of bonding parameters on the copper-solder bonding is presented. Finally, fabrication and assembly processes for the new interconnections approach, based on multi-layer stacking of copper-solder, are developed. The results are analyzed and correlated with the intermetallic growth models to provide optimum process conditions.

Chapter 6 summarizes the work and coherently aligns the results to the research objectives. The chapter closes with suggestions for future work to further develop this innovative interconnection technology.

CHAPTER 2

LITERATURE REVIEW

This chapter focuses on three key aspects of ultra-short interconnection technologies for fine-pitch applications. The main drivers for high I/O density are first discussed, leading to an in-depth study of the state-of-the-art interconnection technologies and the materials, process and manufacturing challenges faced by each. The need for a new copper-solder based technology to fill this technology gap is highlighted in the final part of this chapter.

2.1 Drivers for High I/O Density

Electronics systems can be broadly classified into two main categories depending on their applications, mobile and high-performance systems. The evolution of present day mobile technologies has two main targets: achieving higher logic-to-memory bandwidth while reducing package thickness. High performance systems, on the other hand, are driven by the need to improve the computing speed and the rate of data exchange. High bandwidth, again, is the key enabler here, which has led to a transition from single core towards multi-core processor architectures to achieve high performance.

Bandwidth is defined as the rate of data transfer. Higher bandwidth can be achieved either by decreasing the pitch, which allows for higher amount of data to be transferred, or decreasing the interconnection length, which reduces the time required for data transfer. The ever-increasing bandwidth demand for emerging mobile and high-performance systems has driven the need for newer fine-pitch and ultra-short interconnections technologies. The off-chip interconnection pitches for mobile and high performance systems are projected to reach 20 microns by 2015.

2.2 State-of-the-art Fine-Pitch Interconnection Technologies

The past two decades has seen a continuous evolution in interconnection technologies to address the need for finer pitch. There has been a transition from peripheral wire bonding technology towards area-array flip-chip with solders in the past, copper pillar with solders currently, and pad-to-pad bonding in the future as the requirements for I/O count have increased from a few hundreds to a few thousands, as shown in Figure 4.

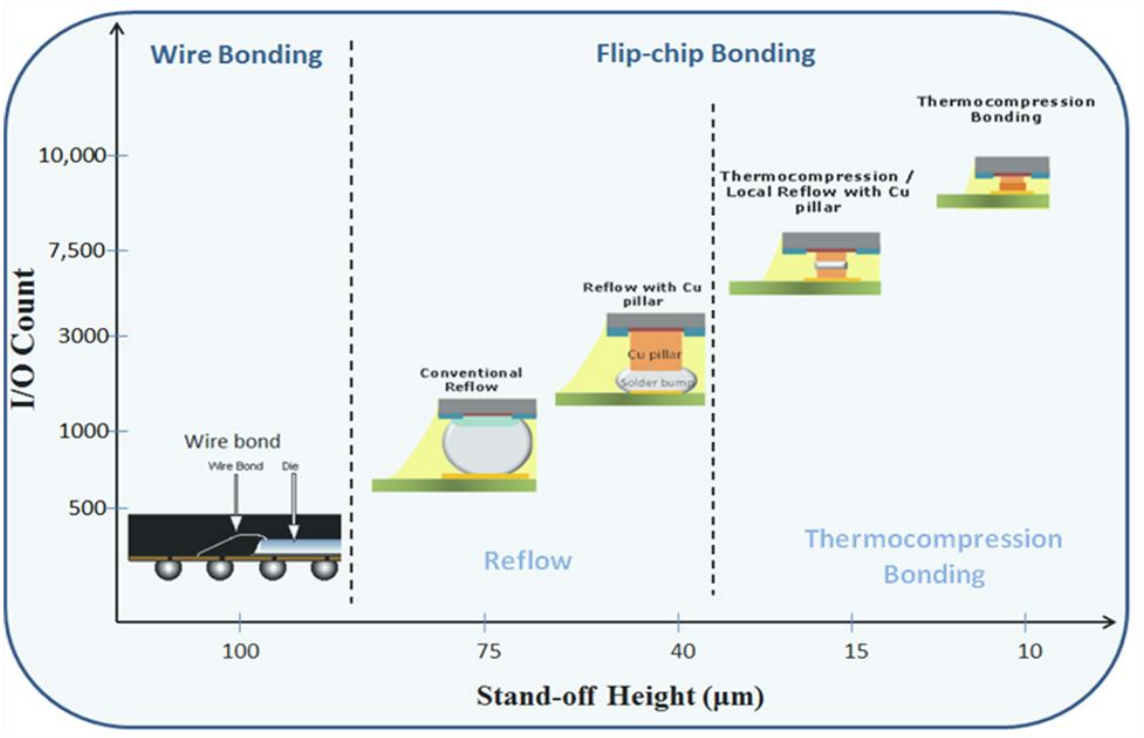


Figure 4: Trend in interconnection technologies with increasing I/O density

Existing off-chip interconnection technologies can be broadly categorized into three main approaches (i) wire bonding with the active side of the chip facing up, (ii) tape automated bonding (TAB) with either of the side of the chip facing up, and (iii) flip-chip, with the active side of the chip facing down. Figure 5 gives a schematic overview of the various approaches that have been used for off-chip interconnections. This sections

initially discusses the limitations of wire bonding and TAB, and then focusses on the state-of-the-art flip-chip technology-based interconnection approaches

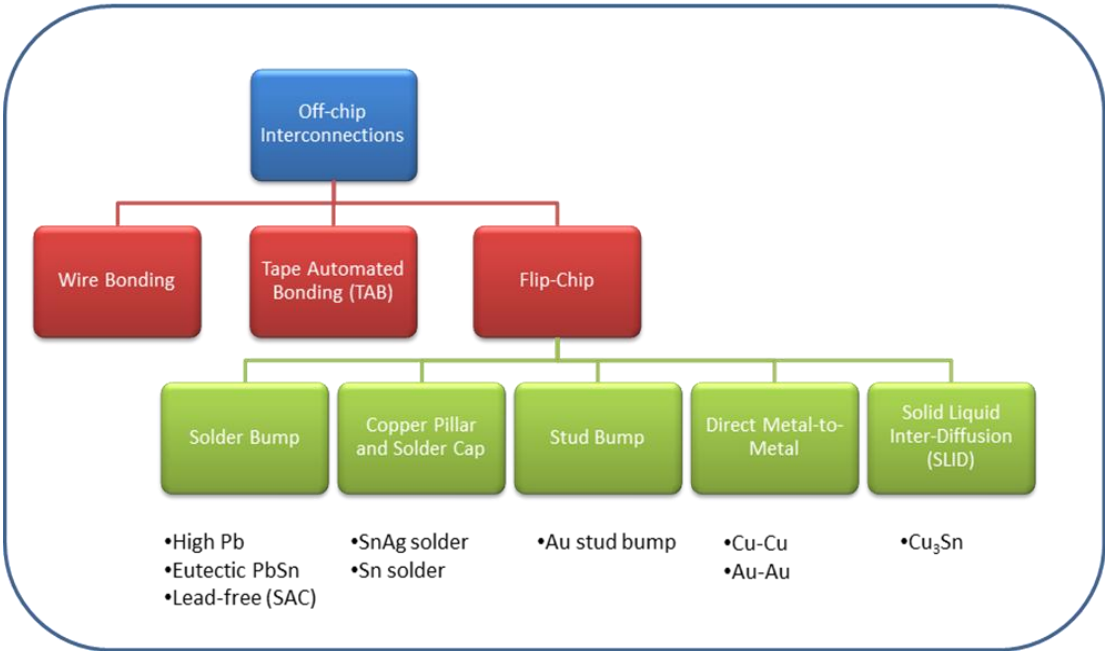


Figure 5: Schematic overview of existing off-chip interconnections approaches

2.2.1 Wire Bonding

Wire bonding is the most primitive and probably the most widely used technology for chip-to-substrate interconnections, and currently accounts for more than 90% of today's chip interconnections. It is also considered as one of the most cost-effective and design-flexible interconnection technologies. Various materials such as gold, aluminum and copper have been used to wire-bond chips due to their excellent malleability, ductility and mechanical properties, ideal for joint formation with thermosonic energy. However, I/O density is limited for these wire-bonded chips as area-array connections are not possible using this method. The long interconnection lengths also degrade the electrical performance due to increased loss, speed and parasitics. Another limitation for this approach is the increased package size in X, Y and Z directions due to larger footprint and large wire-loops. This had led to this technology being restricted to low

performance ICs with low I/O count. Emerging copper wire bonding is capable of achieving interconnection pitches less than 50 microns.

2.2.2 Tape Automated bonding (TAB)

TAB involves placing the bare chip onto the PCB by mounting it first on a flexible polyimide tape. The mounting is done in a way such that the bonding sites of the die are connected to fine conductors on the tape, thus enabling direct connections to external circuits. This allows TAB to handle high I/O counts, while decreasing the stand-off height, thus resulting in thinner packages. This approach provides several advantages over wire bond such as smaller bond pads, higher bond strength, shorter production cycle time, reduced noise and most importantly area-array interconnection capability. At the same time, some of the limitations of TAB are increased time and cost for fabricating the tape and tape-customization required for different chips, increasing package size with increased I/O, high equipment cost and system testability. As a result, TAB is better suited for use in high-volume production applications. Figure 6 shows a schematic of a chip bonded using TAB.

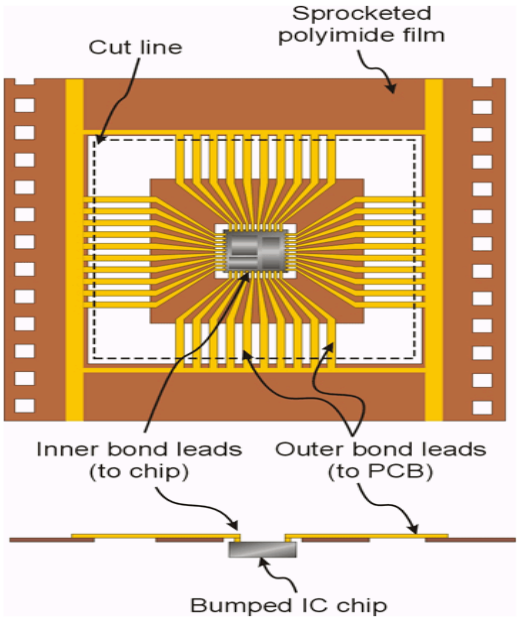


Figure 6: Schematic of chip bonded using TAB

2.2.3 Flip-Chip Bonding

In this method, the chip is directly attached to the substrate with its active side facing down, allowing for peripheral and area-array interconnections, thus providing high I/O density with the shortest electrical path. Thermal performance is also enhanced using flip-chip bonding as the backside of the chip provides a path for heat removal. This approach provides a path towards system miniaturization by reducing the package size. Flip-chip bonding currently enables interconnection pitches of around 30 microns, and this value is projected to decrease to 20 microns by 2015. Flip-chip bonding is projected to be the prevailing technology enabler to achieve the interconnections pitch and density required by emerging applications.

Flip-chip bonding technologies can further be sub-divided based on the materials and processes involved as: (i) Solder bump (ii) Stud bump (iii) Copper pillar and solder cap (iv) Direct metal-to-metal (v) Solid Liquid Inter-Diffusion.

2.2.3.1 Solder Bump

Interconnection technology based on solder-bumps was initially introduced by IBM with their Controlled Collapse Chip Connection (C4) solder bumps. Since its inception, this technology has been the main workhouse for the advancing package performance for more than three decades. Over this period, extensive research has been carried out on the materials and processes associated with solder bumps. Some of the obvious benefits of this technology are low temperature liquid-state bonding and the ability to accommodate non-coplanarity.

Tin-lead solders were preferred because of their low melting temperature range and their excellent wettability, which is attributed primarily to the tin content. Initially solders with high lead (Pb) content were being used (eg. Pb3Sn97). To further decrease the melting point, industry started using eutectic tin-lead solders (Pb63Sn37). An added advantage of eutectic tin-lead solders is their softness, which helps to accommodate

stresses via deformation, thus enhancing the thermo-mechanical reliability of the interconnections. These solders have conventionally been used for interconnection pitches in the range of 80-150 microns. Recently, MCNC (Research Triangle Park, NC) has demonstrated reliable interconnections at 25 micron bump-diameter, 50 micron bump-pitch using eutectic Sn/Pb solder [8].

In February 2003, the "Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment," adopted by the European Union, put a restriction on the use of lead-based solders due to the harmful effects of lead. This forced the semiconductor packaging industry to move to lead-free solders. Sn-Bi solders were explored as a replacement, but the most commonly used lead-free solders are tin-silver (SnAg) or tin-silver-copper (Sn-Ag-Cu), better known as SAC alloys [9]. Tin is the basic soldering element in these solders, while silver and copper contents can be varied depending on the desired mechanical properties. Although the melting point of SAC alloys is about 30-40^{o}C higher than eutectic Sn-Pb, SAC alloys have some advantages such as better thermal fatigue, reliability and substantially higher joint strength.

However, the solder bump technology faces several challenges as the emerging packages demand interconnection at finer pitches. Firstly, shrinking the pitch leads to solder bumps being close to each other, heightening the possibility of solder bridging. The second challenge is that of electromigration, even at moderate current densities, resulting in current crowding, joule-heating and IMC dissolution. Choi et. al. [10] explored the Mean Time To Failure (MTTF) for both Sn-Pb and SAC alloys at 125 micron diameter. The maximum current density and temperature applied to Sn-Pb solder was 2.75×10^4A/cm^2 at 140^{o}C, and that for SAC solder was 3×10^4A/cm^2 at 160^{o}C. The MTTF for Sn-Pb and SAC in these extreme cases was 1 hour and 2 hours respectively. The study concluded that the failure in either case could be attributed to the current

crowding, joule heating and IMC dissolution. Figure 7 shows the void propagation sequence of a SAC solder at a current density of $3x10^4 A/cm^2$ at 140^oC [10].

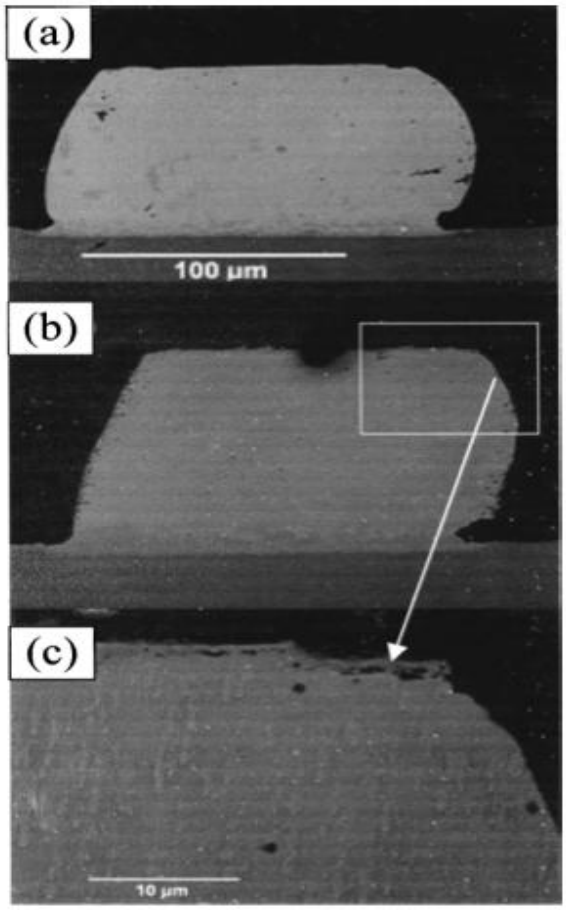


Figure 7: Void propagation sequence of a SAC solder at a current density of $3x10^4 A/cm^2$ at 140^oC [10]

2.3.3.2 Stud Bump

As the use of lead-based solders was prohibited due to environmental regulations, they were replaced with lead-free solders. However, lead-free solders have comparatively higher reflow temperatures, thus creating greater issues with the Under Bump Metallization (UBM) and pitch reduction. As an alternative, stud bumping technology was introduced. Stud bumps, made using copper or gold, can be attached to the substrates using thermo-compression bonding or thermosonic bonding.

In this technique, stud bumps are formed by initially bonding the metallic wire to the substrate by wire bonding, and then snipping the wires just above the formed ball, leading to the formation of a stud. The substrate can then be bonded to the die by thermo-compression bonding with the help of conductive or non-conductive adhesives, or by thermosonic assembly without the use of adhesives [11]. Stud bumping does not require UBM, and thus does not require wafer processing. As stud bumping process is based on wire bonding, the infrastructure for this technology is widely available and process is well known. Interconnection pitches less than 100 microns can be achieved using this approach.

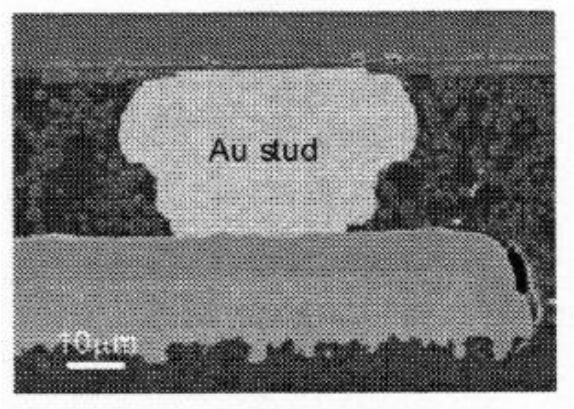


Figure 8: Cross-section of Au stud bump [12]

Gold, being an excellent electrical conductor has high current-handling capability. This was demonstrated by W.S. Kwon et al. [13], who predicted 85μm diameter Au stud bumps with ACF to have a lifetime of 25 years at a current density of $5x10^4 A/cm^2$. As the current density was increased to $7x10^4$ A/cm^2, the lifetime was dramatically reduced to 12.28 hours. Four types of failure mechanisms were found responsible: (i) Au-Al compound formation as a result of Joule-heating, (ii) Al depletion, (iii) cracking at the interface between Au and Au-Al IMC, and (iv) adhesive delamination. However, high cost of gold has become a barrier for manufacturing low-cost packages using this technology. Bump coplanarity is another critical factor required to achieve high yield

using this technology. Also, stud bumping is a relatively slow process as it requires high placement accuracy, and thus is not suitable for dies with high I/O densities due to low throughput concerns.

2.3.3.3 Copper Pillar and Solder Cap

This technology uses a bump structure consisting of a copper pillar with solder deposited on top. The copper pillar brings several advantages. Copper is not only an excellent electrical conductor, but also a good thermal conductor, thus enabling high current-handling. Copper is also compatible with standard BEOL processes and can be scaled down to 1-5 micron pitches without major change in infrastructure. Copper is thus a material of choice to form interconnections at smaller geometries with better electrical performance than achieved with solder bumps. The copper bump keeps the solder bump away from the current-crowding and subsequent joule-heating, thus lowering the bump temperature. The copper bump also prevents solder bridging at finer pitches, while providing additional stand-off height to enhance thermo-mechanical reliability. This technology was first introduced by Intel [14] and APS [15].

A variety of solders have been explored for the solder cap, but the most prominent ones are the SnAg solders [16]. Addition of 2-4% of Ag to the solders helps to inhibit the growth of Cu-Sn IMCs. Tin-silver system has its eutectic point at 3.5% Ag composition, which is the lowest melting composition of SnAg solder. As such, Sn3.5%Ag solder is seen as an attractive option for this technology.

Copper pillar and solder cap approach is capable of supporting pitches as low as 40 microns. IBM has demonstrated reliability of 80 micron and 50 micron pitch interconnections using their copper pillar and solder cap approach, also referred to as Chip Connection (C2) bump technology [17]. Figure 9 shows the cross-section of a C2 flip-chip bump after 1000 cycles of temperature cycling, showing the excellent resistance to thermo-mechanical fatigue of this interconnection technology.

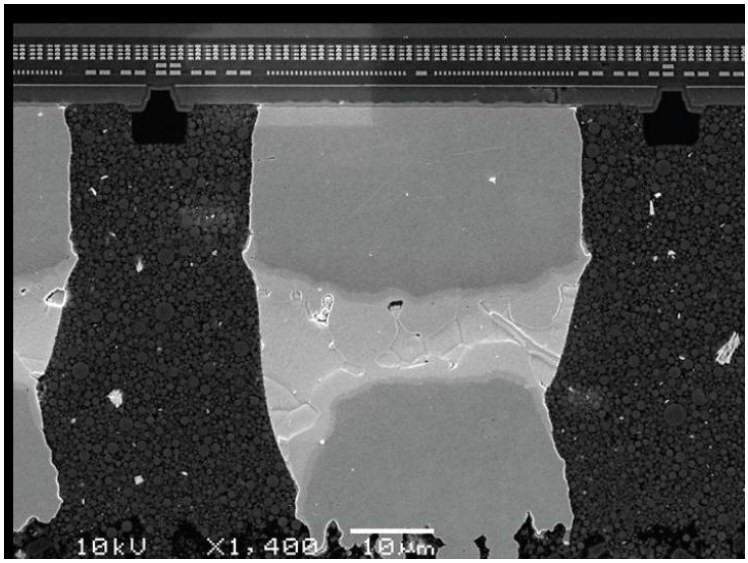


Figure 9: Cross-section of C2 flip-chip bump after 1000TCT [17]

Paik et. al. recently demonstrated reliability of 40 micron pitch Cu-SnAg interconnections with a stand-off height of 20 microns using anhydride-based NCFs [18]. Several steps were taken to optimize the bonding process for such a low stand-off including oxide cleaning before assembly, removal of pressure after mechanical contact of solder on pad and using NCF with optimized viscosity to control solder spreading.

Although copper-solder technology is an improvement over the solder bump approaches due to the excellent electrical properties of copper, it does not get rid of the solder completely, thus facing similar challenges as with solders. Electromigration is a known concern associated with solders because of their low current-carrying capabilities. Zhan et. al. demonstrated electromigration failure for 30 micron pitch, 18 micron diameter Cu-Sn2.5Ag bumps within 350 hours, when exposed to a current of 0.12A at130^{o}C [19]. The failure was induced by dissolution of the Cu/Ni UBM, and current crowding occurred at the entrance of the Al trace into the bump. This failure mechanism was more figurative of solder bumps as compared to copper pillars, reason being the thin UBM. Figure 10 shows the SEM image of these solder micro-bumps after failure.

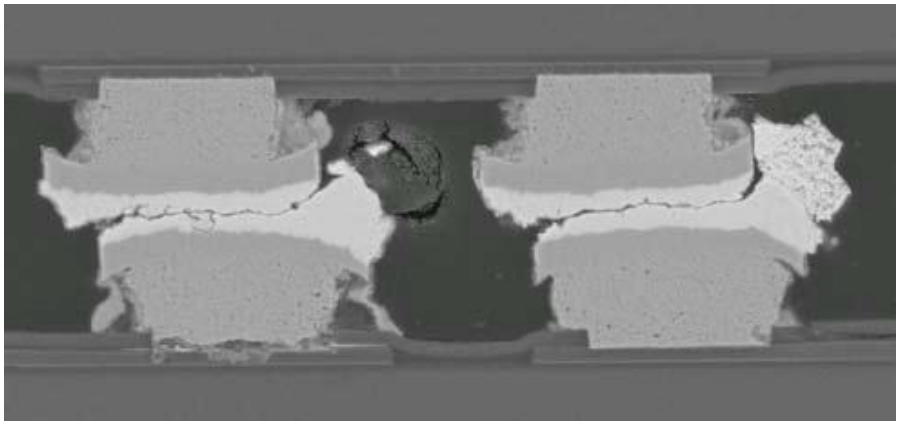


Figure 10: SEM image of Cu/Ni/Sn2.5Ag solder micro-bump interconnect at current stressing of 130^{o}C/ 0.12A for 350 hours [19]

Reliability issues due to the co-presence of solder and IMCs after assembly is another barrier to copper-solder interconnections at finer pitches and lower stand-off heights. IMCs are inherently brittle, and differ remarkably in their properties from solders, which are ductile in nature. Thus IMC formation is a known reason for stress generation in the interconnection bumps. A sufficient amount of solder volume is required to accommodate these stresses developed, and prevent the joints from cracking. Thus, controlling the shape of solder bump, thickness of IMCs, thickness of residual solder becomes very important as interconnection height decreases.

2.3.3.4 Direct Metal-to-Metal without Solder

Metal pads are fabricated from copper and gold at submicron to micron geometries using BEOL or advanced RDL technologies. These can thus be used to fabricate interconnections at 1-20 micron pitch with added benefits such as lower RC delay and better thermal management because of their superior electrical and thermal conductivities compared to solders. Direct metallurgical copper-copper interconnection is therefore being sought after by the semiconductor industry as the “holy grail” or the ultimate goal. However, the major obstacle to the use of these metals in fabricating interconnections is their high melting points. To overcome this, various approaches have

been used involving direct bonding between the two metallic surfaces such as thermo-compression bonding and thermosonic bonding. These bonding techniques rely on solid-state bonding, thus requiring atomic contact between the surfaces, which is obtained either by mechanical deformation or ultrasonic energy. Since both of these approaches involve solid-state bonding, the possibility of bridging is eliminated.

However, direct copper-copper bonding requires smooth and planar bumps, high temperature and long annealing time for inter-diffusion and recrystallization. Low-temperature direct copper-copper bonding requires careful copper surface preparation with Chemical-Mechanical Polishing (CMP) and removal of residual oxides [20]. Further, bonding pressure needed is too high for ultra-high performance devices. Shigetou et. al. demonstrated bump-less copper interconnections at 6 microns pitch by ultra-fine pitch bonding of copper electrodes at room temperature [21]. However, the bonding was performed in vacuum to prevent oxidation post chemical-mechanical polishing, and a novel surface-activated bonder, specially designed for this experiment, was used to accomplish the bonding at such a fine pitch.

The Georgia Tech-Packaging Research Center recently made pioneering advances in low-temperature copper-copper thermo-compression bonding at less than 200^0C, using a manufacturable process without the need for stringent planarity and warpage requirements. HAST, TCT and electro-migration reliability has been demonstrated at 30μm pitch using 10-15μm copper bumps [22]. The 30μm pitch copper interconnections showed stable resistance for more than 1000 hrs even at 10^6 A/cm^2, proving the high current-carrying capability [23]. Figure 11 shows the cross-section of 30 micron pitch copper-copper bonded interconnections using this technology [24].

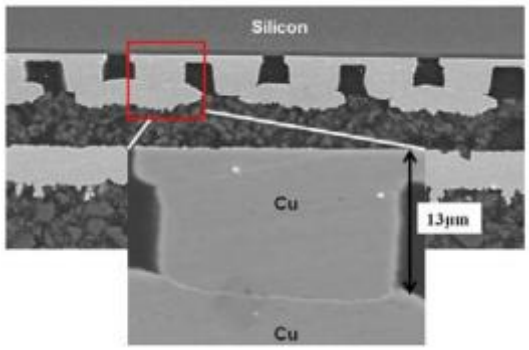


Figure 11: Cross-section of 30μm copper-copper bonding at less than 200^{o}C using NCF [24]

2.3.3.5 Solid Liquid Inter-Diffusion (SLID)

Traditional approaches with copper-solder have shown to have some limitations due to electromigration and thermo-mechanical concerns arising from residual solders. A new technology, referred to as SLID bonding is being explored as a promising approach to overcome some of the challenges previously faced by copper-solder interconnections. SLID bonding is based on the rapid formation of intermetallics between a high melting component (in this case, Cu) and a low melting component (in this case, Sn solder) at a temperature above the melting point of the latter [25]. At this temperature, the copper diffuses into the liquid tin at a very high rate, leading to much faster IMC growth as compared to that in case of solid tin.

Copper forms two intermetallics with tin, namely Cu_6Sn_5 and Cu_3Sn, the latter being the stable IMC. SLID bonding approach involves converting the entire solder volume to the stable IMC, Cu_3Sn, with no residual solder. The final interconnection bump consists of a Cu-Cu_3Sn structure, and is in thermodynamically equilibrium. The melting point of Cu_3Sn is around 670^{o}C. As all the tin is converted to Cu_3Sn, this is the lowest melting point component in the joint, thus making these joints stable up to 670^{o}C. This is of importance as the interconnections are exposed to further reflow steps during

their processing, and a stable compound prevents from further changes taking place in the microstructure.

Wei et al. have examined the electromigration in copper-tin IMCs using edge displacement method [26]. They found that the copper-tin compounds have better resistance to electromigration as compared to eutectic SAC solder. It has also been shown for copper-solder micro-bumps that joints converted to IMCs, either during assembly or current/ temperature stressing, have longer life [27] Labie et. al. demonstrated electromigration testing of 20 micron diameter, Cu-Sn SLID-bonded interconnections at a current density of $6.3x10^4 A/cm^2$ at 150^oC [28]. No failures were observed till 1000 hours of testing. Chang et. al. demonstrated pressure-assisted SLID bonding of 20 micron pitch micro-bumps consisting of a 4 micron copper-pillar and a 4 micron tin-cap structure, using a post-curing step at a temperature of 150^oC for 30 minutes [29]. These interconnections were shown to be reliable over more than 1000 cycles of thermal cycling. Figure 12 shows the cross section of these SLID-bonded interconnection.

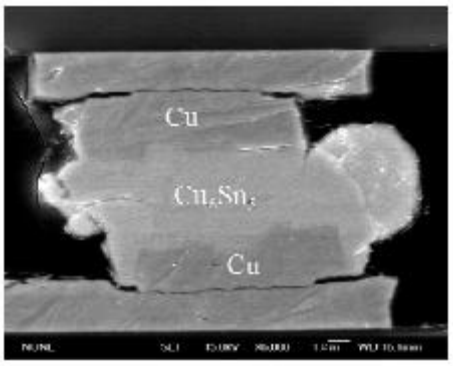


Figure 12: Cross-section of micro-joint formed by SLID bonding [29]

SLID bonding has several advantages over the traditional copper-solder approaches including (i) joint stability over a long range of temperatures, (ii) thermodynamically stable microstructure, which prevents formation of Kirkendall voids, (iii) better electrical performance due to higher electromigration resistance of IMCs as compared to solders. However, diffusion being a slow process, this approach relies on a

long assembly time or generally a subsequent post-annealing step. This leads to a decreased throughput, and makes this approach not truly manufacturable.

Table 2.1 includes a summary of the electromigration analysis completed for all flip-chip approaches mentioned in this section along with the observed failure mechanisms.

Table 2.1: Summary of electromigration analysis for flip-chip approaches

INTERCONNECT APPROACH	BUMP DIAMETER	CURRENT STRESSING CONDITIONS	MTTF	FAILURE MECHANISMS
Solder Bump (Sn-Pb) [10]	125µm	2.75×10^4 A/cm^2 at 140°C	1 hour	• Current crowding • Joule-heating • IMC dissolution
Solder Bump (SAC) [10]	125µm	3×10^4 A/cm^2 at 160°C	2 hours	• Current crowding • Joule-heating • IMC dissolution
Stud Bump (Au) [13]	85µm	7×10^4 A/cm^2	12.28 hours	• Au-Al compound formation as a result of Joule-heating • Al depletion • Cracking at the interface between Au and Au-Al IMC • Adhesive delamination
Copper Pillar and Solder Cap (Cu-Sn2.5Ag) [19]	18µm	1.7×10^4 A/cm^2 at 130°C	350 hours	• Dissolution of Cu/Ni UBM • Current crowding
Direct Metal-to-Metal (Cu-Cu) [23]	30µm	10^6 A/cm^2 at 130°C	>1000 hours	No Failures
Solid Liquid Inter-Diffusion (SLID) (Cu-Sn) [28]	20µm	6.3×10^4 A/cm^2 at 130°C	>1000 hours	No Failures

2.3 Limitations of Current Interconnection Technologies and the Need for a Novel Approach

Solder bump technology has been the preferred approach for flip-chip interconnections for the last two decades. However, solder-bridging and lower current-carrying capability of solder, resulting in electromigration failure due to current crowding, Joule heating and IMC dissolution, limit this technology from going to smaller feature sizes. Although gold is an excellent conductor of electricity, the high cost for bumping, stringent co-planarity requirements, low current-carrying ability of ACF/ ACAs and low throughput for high placement accuracy limits the use of gold stud bumping at finer pitches [30].

In the case of copper-copper interconnection approaches widely pursued by the semiconductor industry, either high temperature (250-400^{o}C) or high pressure (~300MPa) is required to accomplish the bonding. Secondly, complex methods are needed to remove the oxide layer on the copper surface before bonding. Finally, stringent bump coplanarity requirements are needed to ensure bump-to-pad contact throughout the die. These challenges need to be addressed to make this technology a viable option in terms of manufacturability.

The copper pillar and solder-cap approach combines some of the advantages of both copper and solder bump technologies, and is the preferred option from the manufacturability standpoint. However, the current interconnection approaches using this technology are not scalable to finer pitches as a result of electromigration and reliability issues arising with decreased solder content. Solder being a low-strength and low-fatigue resistance material, the solder strains increase with decreased solder height. The formation of copper-tin intermetallics leads to stresses at the IMC-solder interface, which get further aggravated at smaller stand-off heights and lower solder volumes.

Table 2.2 lists the benefits and limitations of the flip-chip interconnections approaches.

Table 2.2: Benefits and Limitations of Flip-chip approaches

INTERCONNECT APPROACH	BENEFITS	LIMITATIONS
Solder Bump	• Low bonding temperature • Ability to accommodate non-coplanarity	• Low current-carrying capability • Solder bridging
Stud Bump	• Available infrastructure • Low bonding temperature • High current-carrying capability	• High cost with gold • Stringent co-planarity requirements • Low throughput for high placement accuracy
Copper Pillar and Solder Cap	• High current-carrying capability compared to solder bump • Fine-pitch bumping	• Electromigration issues at fine pitches • Reliability issues due to solder-IMC co-presence
Direct Metal-to-Metal	• High current-carrying capability • Ultra-fine-pitch bumping	• High bonding temperature OR pressure • Stringent co-planarity requirements • Extensive surface preparation requirement
Solid Liquid Inter-Diffusion (SLID)	• High current-carrying capability • Ultra-fine-pitch bumping • Stable joint composition	• Long assembly times • Brittleness of IMCs

SLID bonding is a promising technology to achieve ultra-fine pitch with a copper-solder system as it relies on the conversion of the entire solder volume into thermally-stable and highly electromigration-resistant Cu-Sn intermetallics. However, IMC formation being a diffusion driven process, long assembly or post-annealing processes are required for such a complete conversion of solders to stable intermetallics. To address this challenge, a novel approach based on multi-layer stacking of copper-solder for high-throughput conversion of solder to stable Cu_3Sn, resulting from decreased diffusion distances is presented in this research.

CHAPTER 3

MODELING AND DESIGN

This chapter initially discusses the finite element analysis performed to determine design guidelines for fine-pitch copper-solder interconnections with low stand-off height. The chapter focuses on the effect of various factors such as solder volume, solder collapse and IMC thickness on the stress distribution in ultra-short copper-solder interconnections after thermo-compression bonding. Based on the predicted stresses, design guidelines are evolved to achieve crack-free assembly with ultra-short copper-solder interconnections. A new approach based on multi-layer stacking of copper-solder is then presented, which will enable ultra-fine pitch low stand-off interconnections with high electromigration resistance. The design for these stacked interconnections is discussed in the second part of the chapter.

3.1 Post-Assembly Stress Distribution in Ultra-short Copper-Solder Bumps

As discussed in the previous chapter, a number of reliability concerns arise from scaling down the interconnection pitch and stand-off height for copper-solder based interconnections. After assembly, intermetallics are formed at the copper-solder interface, which can generate intense internal stresses due to the difference of mechanical properties between IMCs and solder. These internal stresses only intensify during subsequent assembly steps at system level, like lead-free BGA balling and board-level assembly, which contribute to growth of the IMC layer. Reduction of the solder volume limits the capacity of the joints to accommodate these stresses. If the amount of residual solder becomes too little, these internal stresses could result in early failure of the joints after assembly. Careful control of IMC formation and growth during assembly is vital in preventing these early failures. By studying the stress distribution in the bumps, and the

effect of various assembly parameters on the stress, design guidelines will be evolved for the thermo-compression bonding process to minimize the probability of failure.

3.1.1 Design Parameters for Bump Structure

A 2D model was constructed using ANSYS to study the stress distribution in the interconnection bump after assembly. The element used for the model was PLANE183, which is a higher order 2D, 8-node element, and can be used to evaluate plane stresses and strains. Figure 13 shows the location of the nodes for this element. Each node has two degrees of freedom, translations in the X and Y directions.

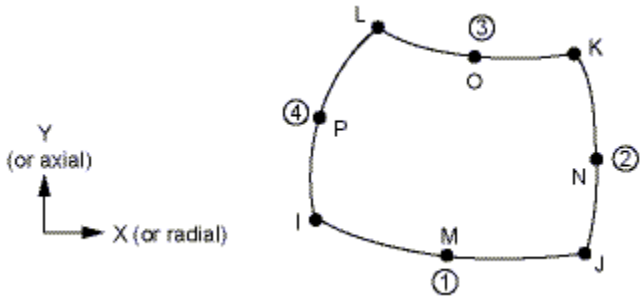


Figure 13: Location of nodes for ELEMENT183

Initially, a single-bump package structure was created, which was then modified to study the effect of different parameters. Since the bumps are axisymmetric, only one-half of the 2D cross-section of the bump was considered. The boundary conditions included constraining the left edge of the package in the X direction and pinning the bottom-most point of the left edge. The package was composed of the silicon die, mounted on a silicon substrate, with a copper re-distribution layer of 3 and 1 micron thickness on the die and substrate side respectively, and the copper-solder interconnection. Silicon was chosen as the substrate material to eliminate the additional stresses arising in the joints due to the CTE mismatch between the die and substrate. Figure 14 shows the ANSYS model of the entire package.

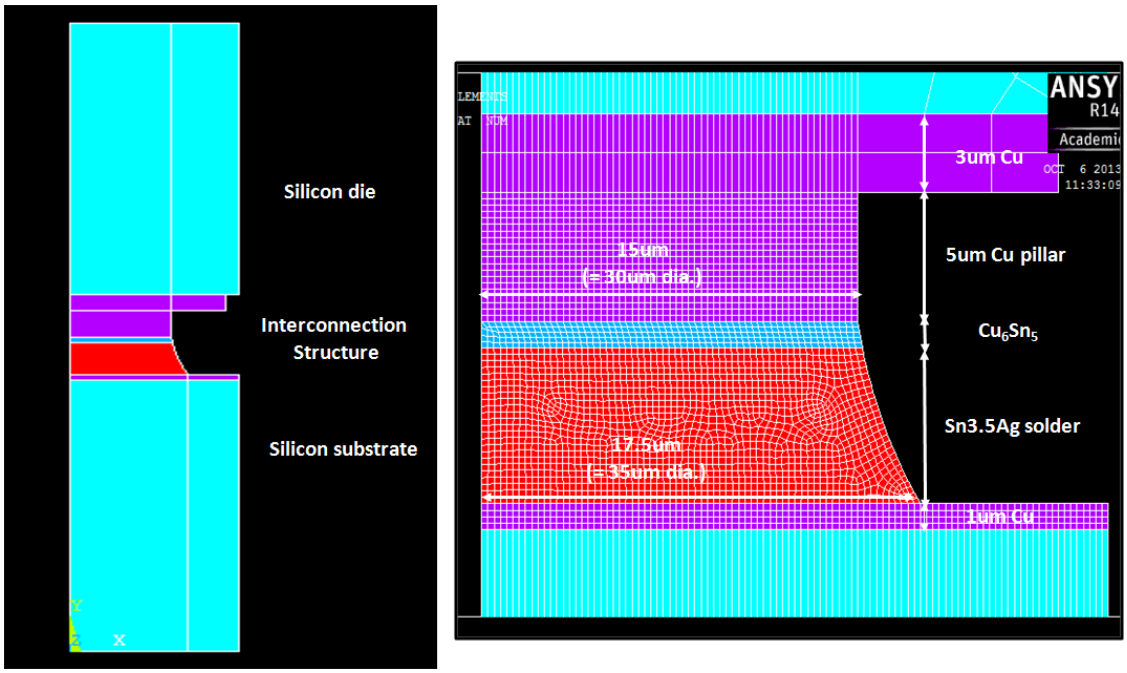


Figure 14: ANSYS model of copper-solder interconnections bump

The ANSYS model closely matched the cross-section of the interconnection in the actual test vehicle, which is described in the next chapter. The interconnection height initially was 15 microns, consisting of 5 microns copper and 10 microns Sn3.5Ag solder. The resultant IMC thickness and residual solder height are a function of the temperature, time and pressure applied during thermo-compression bonding, but are initially set to match the joint-structure resulting from the initial assembly process of record (POR). The only IMC considered is Cu_6Sn_5, as the amount of Cu_3Sn formed is negligible for the bonding temperature and time, as has been confirmed through Energy Dispersive X-ray Spectroscopy (EDS). The pressure also controlled solder collapse on the substrate landing pads to a certain extent. The materials and properties for the die, substrate and interconnection structure were kept constant throughout this study. The SnAg solder alloy is a visco-plastic material, and its stress-strain behavior follows the constitutive Anand model, classically used to extensively account for both, plasticity and creep effects. Table 3.1 lists the material parameters of Anand Model for Sn3.5%Ag solder.

Table 3.2: Material Parameters of Anand Model for Sn3.5%Ag

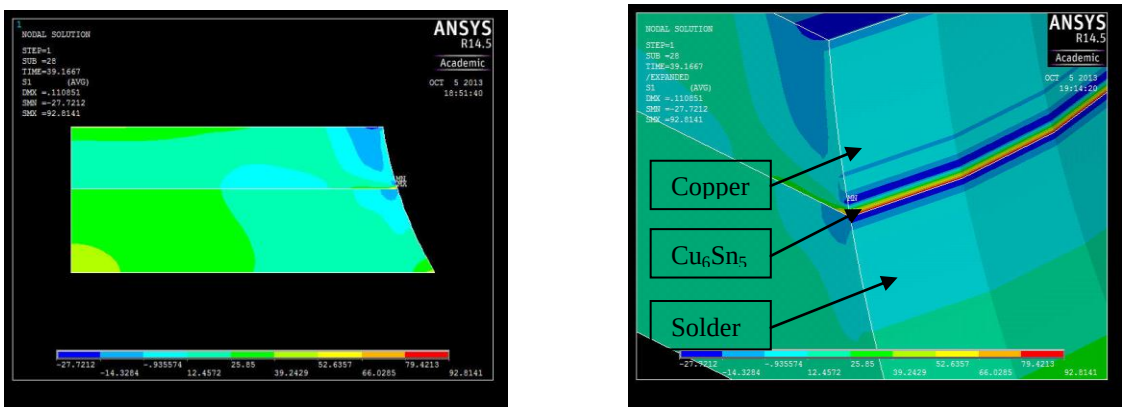
PARAMETER	SYMBOL	VALUE
Pre-exponential factor	A (sec^{-1})	177016
Activation Energy	Q (J/mol)	85459
Coefficient (constant)	$\hat{S}$ (MPa)	52.4
Hardening/ softening constant	h_0 (MPa)	27782
Stress multiplier (material constant)	ξ	7
Strain rate sensitivity	m	0.207
Material constant	n	0.0177
Material parameter	a	1.6

The other parameters used to define the materials were the Young's modulus, Poisson's ratio and the Coefficient of Thermal Expansion (CTE). Table 3.2 lists these material properties used for modeling the interconnections.

Table 3.2: Material Properties used for ANSYS modeling

MATERIAL	ELASTIC MODULUS (GPa)	POISSON'S RATIO	CTE (ppm/^{O}C)
Silicon	120	0.28	2.7
Copper	121	0.3	17.3
Sn3.5Ag solder	52.4	0.34	21.85
IMC (Cu_6Sn_5)	120	0.3	16.3

After building the model, it was free meshed into squares with dimensions of 0.25 microns. Residual stresses in interconnects are mostly generated during the cooling-down phase of solder reflow due to the mismatch in the mechanical and thermo-mechanical properties of the stack-up materials. The structure was considered stress-free at 260^{o}C, and its temperature was uniformly ramped down to 25^{o}C in 100 seconds to emulate the cool-down phase. Figure 15 shows the distribution of principal stresses across the interconnection structure after assembly.



(a) **(b)**

Figure 15: Principal stress distribution in the bumps post assembly reflow (a) 2D view (b) Axisymmetrical expansion view

Stress concentration was, as expected, observed at the edge of the interface between the solder and IMC. Apart from this point, there was no obvious stress concentration. Depending on the amount of stress generated, and the strength of the materials, this stress concentration could lead to crack initiation and propagation, resulting in failure of the joints. Effect of various factors such as solder height, IMC thickness, solder collapse and cooling rate on the stress distribution was studied, so as to optimize the assembly process to prevent early failures of the joints.

3.1.2 Effect of Solder Height on the Internal Stress in the Interconnections

As the diffusion rate is independent of volume, the thickness of the IMC layer formed during assembly does not depend on the solder height of the bumps. Thus, for any defined assembly process, the residual solder height is determined by the initial solder height. The joint height has a significant effect on the internal stress developed in the interconnections. Hence, it is important to evaluate how internal stresses evolve with the height of residual solder, so as to determine the minimum solder volume required for a reliable interconnection structure.

With a fixed IMC thickness of 3 microns, the initial solder (residual solder) height was varied from 5 to 15 (2 to 12) microns, and the maximum principal stress at the solder-IMC interface was compared. The curvature of the bump was kept constant in each case. It was found that the maximum stress decreases with increasing height of the initial solder (residual solder), as seen in Figure 16. As can be seen from the Figure 17, there is a minimum solder height of 10 microns, required to obtain a low stress level in the joints, and the stress shows little variation with further increase in the solder height.

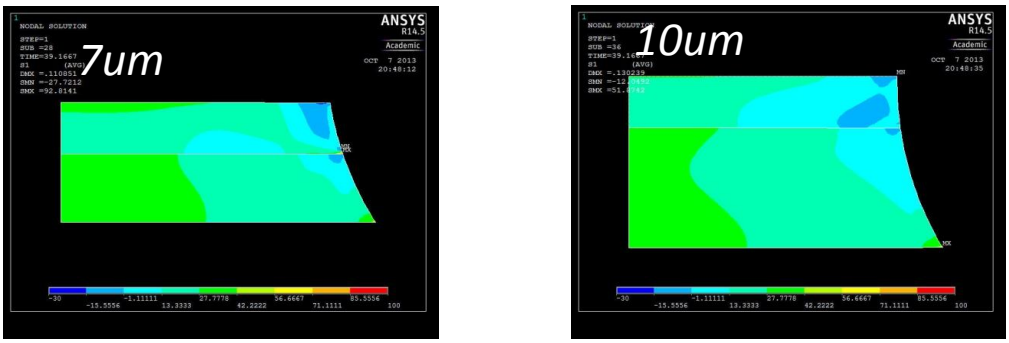


Figure 16: Principal stress distribution in the bumps after assembly with varying solder heights

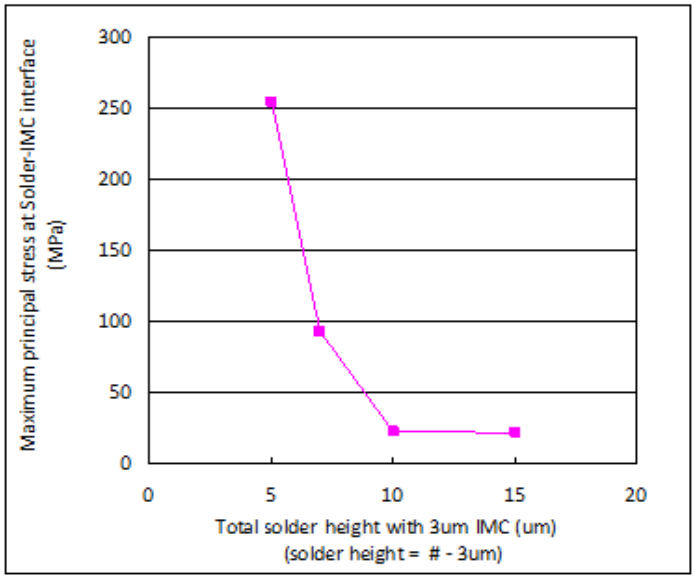


Figure 17: Effect of varying solder height on the maximum principal stress at solder-IMC interface

3.1.3 Effect of Solder Collapse on the Internal Stress in the Interconnections

Pressure applied during thermo-compression bonding, controls the extent of solder collapse to a certain extent. This solder collapse is further enhanced due to the excellent wettability of the palladium finish on the substrate, and fluxing agents in the B-staged No-flow Underfill (BNUF) used in this research. The joint-shape, which results from the solder collapse, is also known to have an influence on the internal stress generation in the bumps. Keeping the solder volume and the IMC thickness (3 microns) constant, the bottom diameter of the joint was varied between 30 and 45 microns, and its impact on the maximum principal stress at the solder-IMC interface was studied. It was observed that increasing the bottom diameter of the joint results in an increase in the maximum principal stress at the solder-IMC, as seen in Figure 19. Increased solder collapse also results in decreased height of the residual solder. It can be concluded that the solder collapse during assembly should be kept to a minimum to reduce the internal stress generated in the joints. Thus, the applied pressure needs to be optimized, so as to have little solder collapse, while still accommodating the variation in the bump heights.

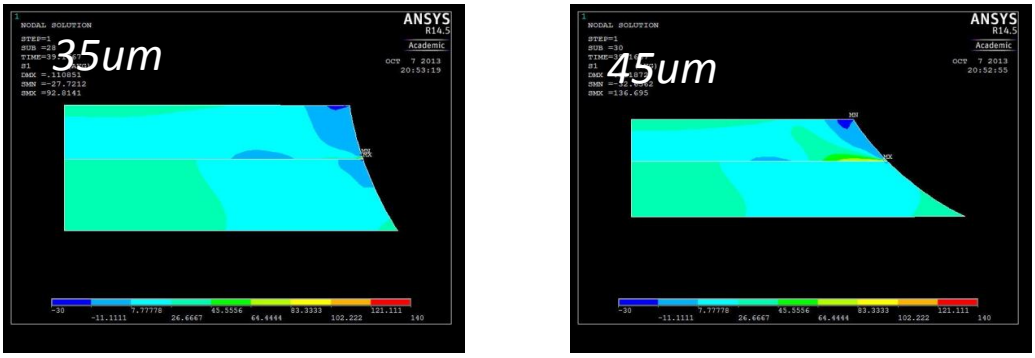


Figure 18: Principal stress distribution in the bumps post assembly with varying solder collapse

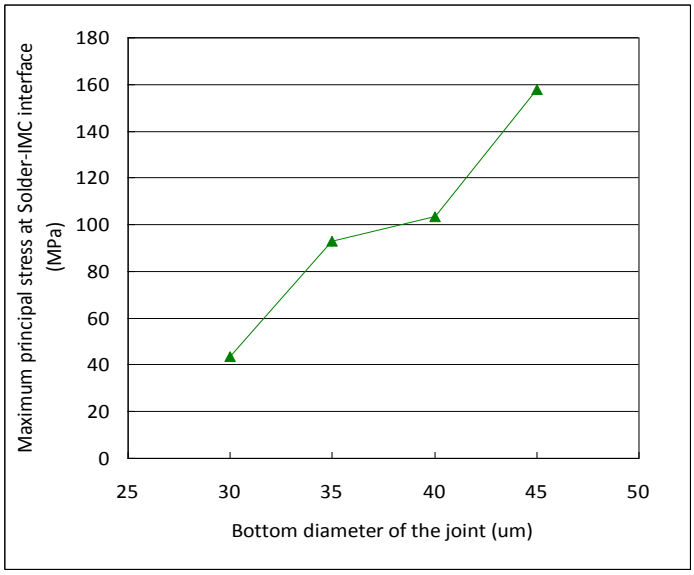


Figure 19: Effect of solder collapse on the maximum principal stress at solder-IMC interface

3.1.4 Effect of IMC Thickness and Cooling Rate on the Internal Stress in the Interconnections

Another source for stress generation in the interconnection bumps is the difference in mechanical properties of the solder and IMCs. The effect of increasing IMC thickness on the stress was studied. Intermetallic formation, being a diffusion process, the thickness of IMC (Cu_6Sn_5) in the joint is determined by the temperature and time of bonding. At a constant joint height of 8 microns, it was observed that the maximum stress at the solder-IMC interface increases as the IMC thickness in the bumps increases from 0.5 microns to 5 microns, but decreases with a further increase in the IMC thickness.

For joints with low IMC content, the solder is responsible for accommodating the internal stress in the interconnections. As the intermetallic content of the joint increases beyond a limit, the stress accommodation is mainly driven by the capacity of the IMCs to absorb it. SLID bonding, which involves converting all of the solder to stable intermetallics, eliminates all the residual stress, thus improving reliability of the joints.

The effect of cooling rate on the maximum stress was also studied. A fast cooling rate leads to increased residual stresses, and this was also observed from the finite

element analysis. Two different cooling rates, 1K/sec and 6k/sec were used, and the faster cooling resulted in about 10 percent higher stresses. Both these trends are shown in Figure 20 below.

As cooling rate increases, the stress in the residual solder increases. However, the variation of the stress with cooling rate is small. A slow cooling rate corresponds to a longer time at higher temperatures, resulting in a thicker IMC layer, and thus higher stress. The effect of a thicker IMC layer is greater than that of a slower cooling rate. Moreover a slower cooling process also results in a higher thermal budget. Therefore, a faster cooling process is preferred for bonding of copper-solder interconnections.

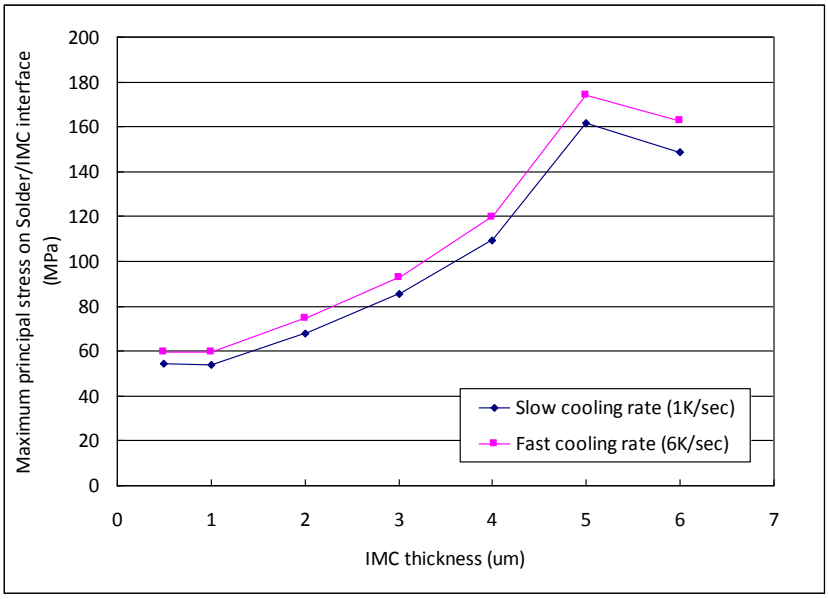


Figure 20: Effect of varying IMC thickness and cooling rate on the maximum principal stress at solder-IMC interface

3.1.4 Design Guidelines for Ultra-short Copper-Solder Interconnections

Based on the modeling results, the guidelines drawn for thermo-compression assembly with ultra-short copper-solder interconnections include assembly and design optimization with: (i) initial solder height of 10 microns to maintain low level of stress in the joints, (ii) optimized pressure to control solder collapse, while accommodating the

bump height variation, and (iii) fast cooling rate during assembly, to reduce IMC thickness and thus the internal stress in the joints.

The internal stress plays a critical role in the reliability of the interconnections, and may induce early failures. Thus, there is a need to control the IMC formation and growth through process optimization or by introducing a barrier layer. Another option to tackle this issue involves converting the entire joint structure to stable intermetallics using SLID bonding. However, intermetallic formation, being a diffusion-driven process, requires long assembly times or post-annealing processes.

3.2 Design for Ultra-short Fine-Pitch Copper-Solder Stacked Interconnections

A new copper-solder interconnections approach was proposed to overcome the challenges of ultra-short interconnections at fine pitches. This approach is based on combining SLID bonding with a multi-layered copper-solder bump structure to achieve higher diffusion rates through reduced diffusion distances, resulting in much faster conversion of solder to intermetallics. This innovative multi-layer copper-solder stack approach can be used to achieve fine-pitch off-chip interconnections, which are capable of handling high current-densities. Interconnections using this new technology also enable high throughput assembly with high yield, even at low stand-off heights. A schematic of the bump structure for this approach is shown in Figure 21.

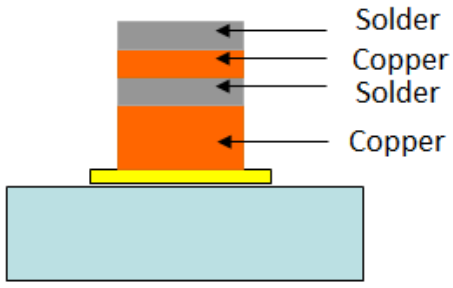


Figure 21: Proposed bump structure for copper-solder stacked interconnections approach

The fundamental innovation in this technology is the stacking of multiple thin layers of copper and tin, which help to decrease the diffusion distances. This leads to faster IMC formation, resulting in conversion of solder to IMCs at much lower bonding temperatures and times, than those used in traditional SLID bonding.

3.2.1 Physical Design of the Stacked Structure

Presence of silver in the solder inhibits the formation of intermetallics to some extent. Since this approach requires faster formation of intermetallics, pure tin was used as the solder. Based on the atomic weights and densities of copper and tin, the minimum thickness ratio of the copper and tin layers was calculated to be 1.3 for conversion of tin to Cu_3Sn.

Ideally, the thickness of individual copper and tin layers should be as small as possible for lowest diffusion distances. This, however, is restricted by the process capability for copper and tin electroplating. Also, a very thin layer of tin results in insufficient wetting, due to instant solidification of the tin upon melting. From previous literature, it was observed that the tin thickness used for SLID bonding is usually in the range from 1-4 microns. Based on the process capability of the available copper and tin electroplating setup, a 1.5 microns thick tin layer was chosen for the bump structure. Using the thickness ratio previously calculated, the corresponding thickness of the copper layer was 2 microns.

The thickness of the initial copper layer was chosen to be 5 microns as this layer is responsible for providing adhesion to the seed layer, and as such, cannot be completely consumed to form IMCs. For the final tin layer, the thickness was chosen to be 3 microns to ensure all bumps land on the substrate. A total of three layers each of copper and tin were chosen to be stacked alternately, resulting in a final bump height of 15 microns.

Figure 22 shows the final configuration of the bump for the copper-solder stacked interconnections approach.

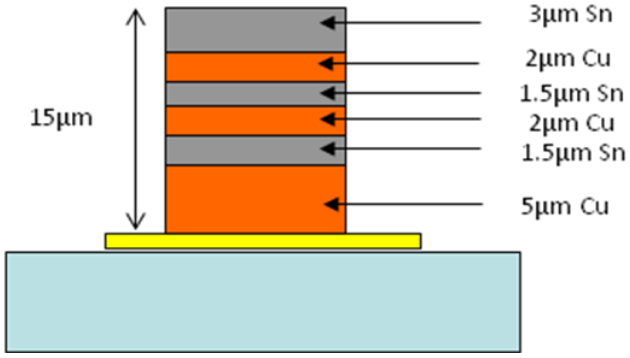


Figure 22: Bump configuration for copper-solder stacked interconnections

3.2.2 Diffusion Modeling of Copper-Tin Stack

Intermetallic formation between copper and tin is a diffusion-limited process. As such, the IMC formation can be modeled using a parabolic law which is based on Fick's first law of diffusion, where the inter-diffusion coefficient can be calculated using the Arrhenius relationship. The parabolic law used and the Arrhenius relationship are shown in Figure 23.

$$\Delta x^2 = k \cdot t$$

$$k = k_0 \exp\left(-\frac{Q}{RT}\right)$$

Δx = thickness of Cu_3Sn after time t
k = inter-diffusion coefficient

k_0 = intrinsic diffusivity
Q = activation energy
T = temperature

Figure 23: Expressions for the parabolic growth law and Arrhenius relationship

The assumptions made while simulating the intermetallic growth were (i) constant concentration of the diffusing species at the inter-layer boundaries, and (ii) constant concentration-gradient along the inter-layer. Values for the activation energy for the formation of Cu_3Sn (Q) and its intrinsic diffusivity (k_0) were taken from previous studies

based on the growth of copper-tin intermetallics. These values differ with processing techniques, and the values selected for this study were applicable to thin films of copper and tin. The 'Q' and 'k_0' values used were 66.1 kJ/mol and 5.3E-8 m^2/s respectively.

Modeling the IMC formation is of importance as it provides an estimation of the bonding temperature and time needed for complete conversion of solder to Cu_3Sn using the above bump configuration. Based on the parabolic law, Arrhenius relationship and the values for 'Q' and 'k_0' it was calculated that 2 microns of Cu_3Sn could be formed in 300 seconds at a temperature of 250^0C. Since the thickness of the tin layers in the bump structure was 1.5 microns, they would be completely converted to Cu_3Sn at a bonding temperature and time of 250^0C and 300 seconds respectively.

CHAPTER 4

EXPERIMENTAL PROCEDURES

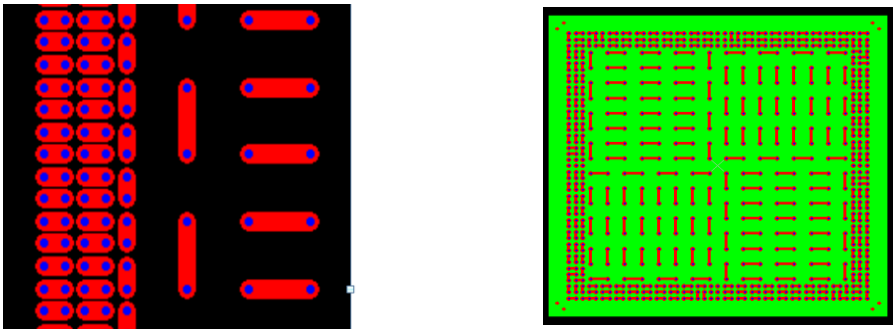
This chapter describes the materials and the processing techniques used to fabricate the 50 and 100 micron pitch ultra-short copper-solder interconnections. The chapter starts with a description of the test vehicle design for this research. An in-depth description of the fabrication processes for the dies and substrates then follows. The chapter ends with descriptions of the assembly process for these interconnections and the characterization techniques used during the course of this research.

4.1 Test Vehicle Design

Two different test vehicle designs, as shown in Figure 24, were used for this research. Test vehicle A consisted of a 10mm x 10mm die design with 7071 bumps having two variations, 15 microns and 30 microns bump diameters. The minimum pitch for this test vehicle was 50 microns. Test vehicle B had a 5mm x 5mm die design with 760 bumps of 30 or 50 microns diameter. The minimum pitch for test vehicle B was 100 microns. Both these designs consisted of a peripheral array of interconnections at the minimum pitch and an area array of interconnections at a relatively coarser pitch.

Table 4.1: Design parameters for test vehicles A and B

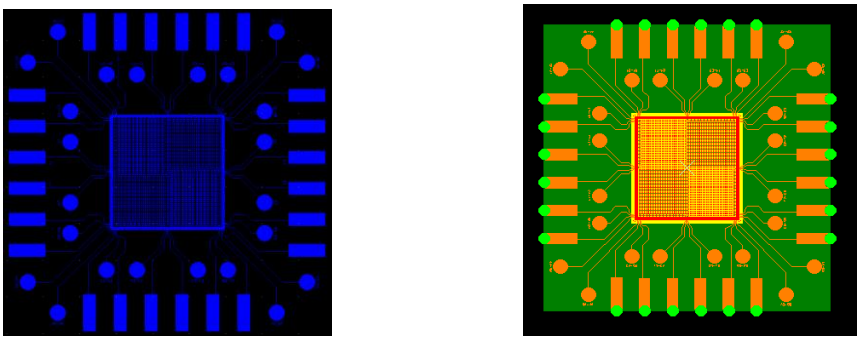
PARAMETER	VALUE (TV A)	VALUE (TV B)
Interconnect pitch	50µm	100µm
Number of I/Os	7071	760
Die size	10x10 mm^2	5x5mm^2
Bump diameter	15/ 30µm	30/ 50µm
Bump height	15µm	15µm



A **B**

Figure 24: Die designs showing bump layout for test vehicles A and B

Daisy-chain patterns were incorporated within each die to assess the reliability performance of these interconnections in Highly Accelerated Stress Test (HAST) and High Temperature Storage (HTS) test. To form these daisy chains, the die pads on the substrate were connected in a way which was complementary to the routing layer in the die. Apart from the daisy chains, Kelvin test structures were also provided in the test vehicles to measure single bump resistance of the four corner bumps, as these bumps are expected to be the first ones to fail. Probing pads provided on the substrates help to measure the single bump as well as the daisy chain resistance values. Fiducials were provided on the dies and substrates to assist with alignment during assembly.



A **B**

Figure 25: Substrate designs for test vehicles A and B

4.2 Die Fabrication

Dies were fabricated on 4” and 6” silicon wafers having a thickness of 400 microns. The wafer fabrication was a two-mask process. The first mask was used to define the routing layer on the chip-side to form the daisy chain. The second mask defined the interconnection bumps, where each die pad footprint matched with the substrate for the subsequent assembly step. Figure 26 gives an overview of the wafer fabrication process.

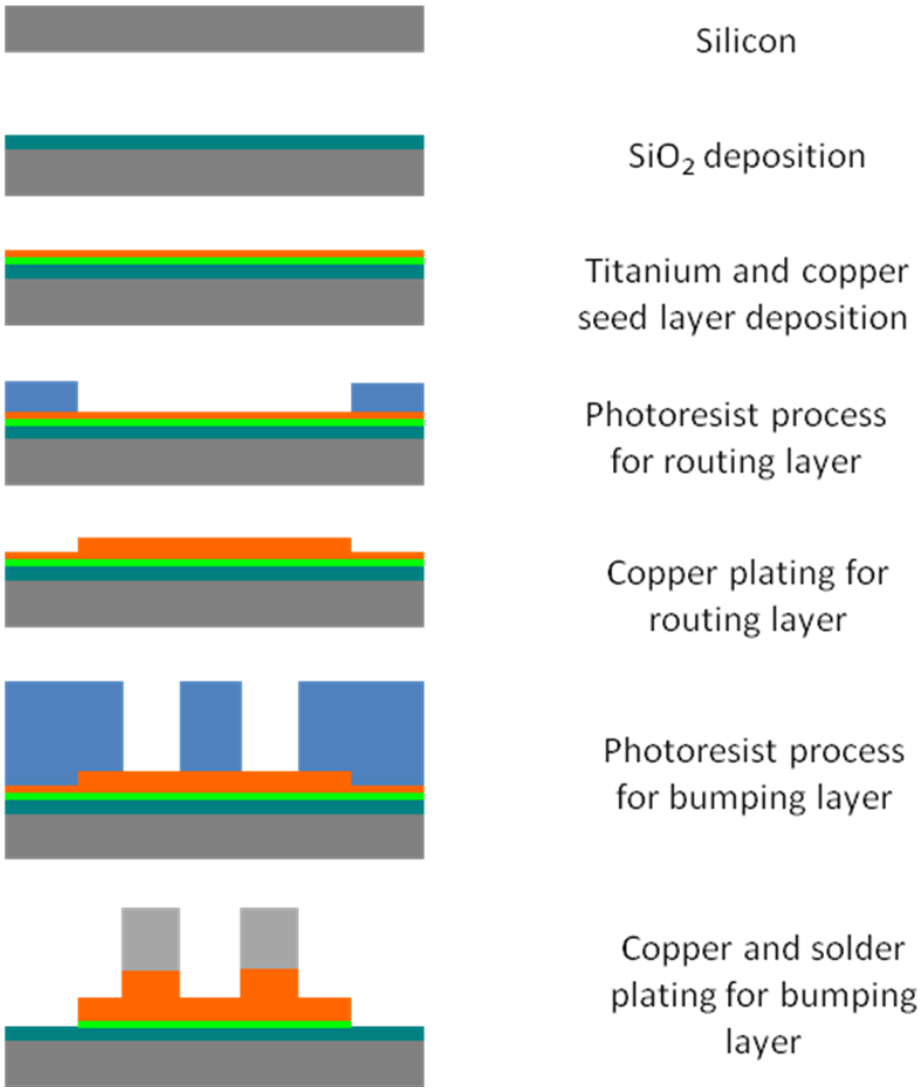


Figure 26: Overview of wafer fabrication process

The standard semi-additive process was used to fabricate the dies. Initially, the wafers were cleaned using the standard CMOS processes to remove the surface contaminants. This included keeping the wafer in Piranha solution (3:1 mixture of conc. H_2SO_4 and 30% H_2O_2) for 20 minutes at 120^oC and then rinsing with de-ionized water.

4.2.1 Insulation and Seed Layer

An insulation layer of silicon dioxide (SiO_2) was initially deposited using plasma-enhanced chemical vapor deposition (PECVD). This layer serves as insulation between the conductive silicon and the subsequent conductive layers built on top of it.

Table 4.2: Parameters for insulation layer deposition

PARAMETER	VALUE
Power	50W
Temperature	250^oC
SiH_4 flow rate (sccm)	400
N_2O flow rate (sccm)	900
Deposition rate	50 nm/min
Deposition time	20 min

DC magnetron sputtering was used to deposit a 40-50nm titanium (Ti) layer, and then a 400nm thick copper seed layer. The Ti layer acts as adhesion layer between the SiO_2 and the copper seed layer. The copper seed layer was created for subsequent electroplating of the routing layer and bump structures.

Table 4.3: Parameters for seed layer sputtering

PARAMETER	VALUE
Titanium	
Power	340W
Current	1.4A
Deposition rate	1 A/sec
Deposition time	8 min
Copper	
Power	1000W
Current	2.4A
Deposition rate	8 A/sec
Deposition time	6 min

4.2.2 Metal Routing Layer

The routing layer, also referred to as the 'dog-bone' layer, is equivalent to the redistribution layer which serves as a pad for the copper bumps. The pattern for the first metal routing layer was created using photolithography. Hitachi RY-5315EB negative dry film photo-resist having a thickness of 15 microns was used for lamination. The wafers were exposed using the Karl-Suss MA6 Mask Aligner, under hard contact, with a dose of 95mJ/cm^2 and then developed in 3% Na_2CO_3 solution at 85^{o}C for 2 minutes.

Even after the wafers are rinsed thoroughly after developing, some organic residue is left at the interface between the copper seed layer and the resist that will prevent adhesion of the electro-deposited copper to the seed layer. The wafers were cleaned of this residue by performing O_2 plasma descum using a Reactive Ion Etching (RIE) tool. At this stage the wafers were ready for electroplating.

Table 4.4: Parameters for plasma treatment

PARAMETER	VALUE
Temperature	100^{o}C
Plasma Gas	O_2
RF Power	400W
Plasma Time	5 mins

Copper plating for the routing layer was performed using an in-house copper plating bath containing Cupracid TP chemistry. Table 4.5 lists the bath components.

Table 4.5: Components of copper electroplating bath

MAKE UP OF 100L	VALUE
DI Water	Approx 65 liters
Copper(II)-sulfate-5-hydrate	6.0 kg
Sulfuric acid, chem. pure (50 % w/w)	32.1 liters
NaCl (chemically pure)	0.012 kg
Cupracid TP Leveler	2.0 liters
Cupracid Brightener	0.2 liter
Cupracid Starter	0.2 liter

Initially, a dummy board, coated with copper, was inserted in the copper bath and plated at 8A for 20 minutes. After ensuring good quality plating, the actual wafers were put in the bath for plating of the routing layer. The wafers were framed to a square rack to secure them during the electroplating process. This is shown in Figure 27 below.

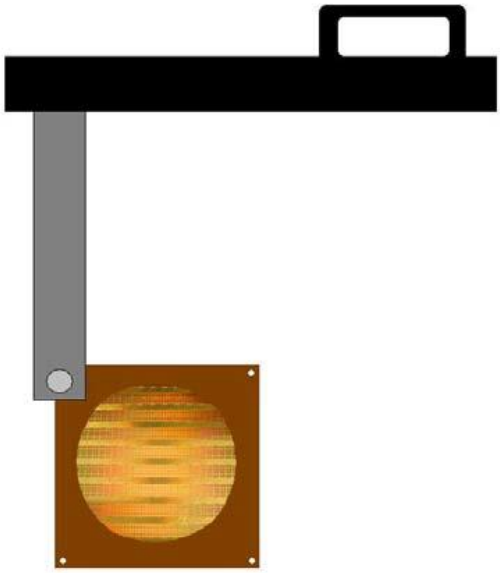


Figure 27: Rack to hold wafer during copper electroplating

The area of the frame (~400cm^2) dominates the wafer area to be plated (~15cm^2). Thus a current of 6A was used, resulting in a current density of 15mA/cm^2 for the 4" wafer. The thickness of the routing layer was about 3 microns, which was determined using a Dektak profilometer. The orientation of the wafers in the frame was changed periodically to ensure uniform plating across the wafer.

Table 4.6: Parameters for copper electroplating

PARAMETER	VALUE
Temperature	23^{o}C
Current density	15 mA/cm^2
Deposition rate	0.33 μm/min
Deposition time	9 min

After the plating process, Enthone PC 4025 stripper was used to strip the dry film photoresist. The wafers were immersed in the stripper solution at 35-45^{o}C for 30-60 sec, during which time they were agitated to ensure complete removal of the photoresist. The wafers were then cleaned using 10% H_2SO_4 to remove any remaining organic residue.

4.2.3 Metal Bumping Layer

The process for forming the pattern for the bumps was fairly similar to that of the routing layer. Photolithography was used to pattern the bumping layer. The same Hitachi dry film 15 microns photoresist was used for lamination. Glass masks with the bumping layer design were used for exposure. Alignment of the mask with the routing layer design was an important step in this process. The wafers were exposed using the Karl-Suss MA6 Mask Aligner tool under hard contact, and received a dose of 95mJ/cm^2. They were then developed in 3% Na_2Co_3 solution at 85^{o}C for about two minutes. After developing, the wafers were cleaned for organic residues using the O_2 plasma descum treatment.

The interconnection bumps have a total height of 15 microns, which consists of 5 microns of copper and 10 microns of SnAg solder. The same in-house copper plating bath was used to electroplate the copper. A current density of 15mA/cm^2 was used, which resulted in a deposition rate of 0.33μm/min. The deposition time was 15 minutes, and again the orientation of the wafers was periodically changed to ensure uniform plating. Solderfill AG800 chemistry, provided by Atotech was used for electroplating the solder. The anode for the solder plating process is a titanium iridium mesh, which is an inert electrode. The bath was not agitated during the plating, which resulted in slight foaming.

Before plating the wafers, a dummy board was immersed into the solder bath and plated at 2A for 20 minutes. This was done to ensure good quality plating. After this, the wafers to be plated were immersed in the bath using alligator clips. A current of 0.23A was set based on the active area of the wafers (~15cm^2), in order to maintain a current density of 15mA/cm^2. This value of current density was selected so as to deposit the

desired eutectic composition of solder, Sn3.5%Ag. The resultant deposition rate was 0.75µm/min. The total bump height was 15 microns, which was measured using the Dektak Profilometer.

Table 4.7: Parameters for SnAg solder electroplating

PARAMETER	VALUE
Temperature	20-25^{o}C
Current density	15 mA/cm^{2}
Deposition rate	0.75µm/min
Deposition time	~13 min

The wafers were immersed in the stripper solution at 35-45^{o}C and agitated for 30-60 sec to remove the photoresist. The next step was the etching of the seed layer. Copper seed layer was removed by immersing the wafer in copper etchant (1:3:30 solution of H2SO4: H2O2: H2O) for 30 sec. Titanium layer was removed using 5% dilute HF acid for 5 sec. At this stage the wafers were ready to be diced into individual dies, which then were used for assembly. Figure 28 shows images of the fabricated copper-solder bumps taken using the Zeiss SEM.

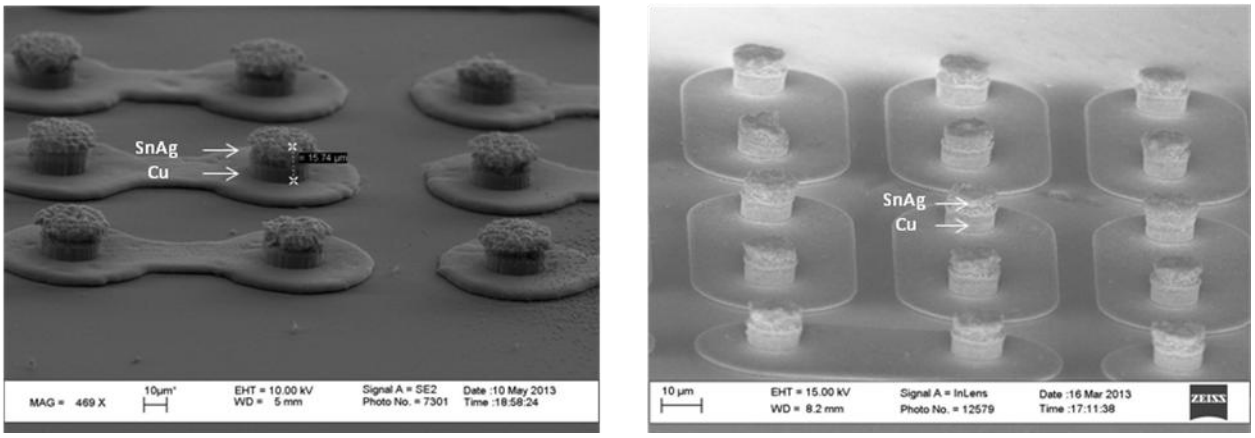


Figure 28: SEM images of fabricated copper-solder bumps

4.3 Substrate Fabrication

The fabricated dies were assembled onto substrates to study the reliability of the fine-pitch copper-solder interconnections. Silicon and glass were used as substrate materials as part of this study. Silicon (3ppm/^{o}C) and glass (3.8ppm/ ^{o}C), because of their low CTE mismatch with silicon dies, help in eliminating warpage of the substrate, and the resultant substrate non-coplanarity, and thus improve the yield and reliability of these interconnections.

Glass has several other advantages over organics, which make it a promising substrate material. It has excellent electrical properties because of its low dielectric constant and loss tangent. Due to its low CTE, glass shows high dimensional stability up to 500-600^{o}C. It demonstrates high resistance to process chemicals. Another advantage of glass substrates is their transparency, which proves useful during die-substrate alignment for assembly. Importantly, large ultra-thin glass panels can be manufactured at very low costs.

For this research, substrates were fabricated with a semi-additive process. The baseline process for fabrication is shown in Figure 29.

The first step was cleaning the 100 micron thick glass with acetone, iso-propanol and then DI water. This was followed by silane treatment, which is used as a surface finish to improve adhesion of the build-up polymers. A ZIF build-up layer of 17.5 microns thickness was then laminated on either sides of the glass with the help of a vacuum laminator. ZIF was used as the build-up dielectric because of its ultra-smooth surface, low RF power loss during transmission and high insulation reliability. Copper was then plated on the build-up layers using electroless plating. This would act as the seed layer for subsequent copper electroplating.

Patterning of the substrates was done using 15 microns-thick Hitachi RY-5315EB dry-film photoresist. Initially, photoresist was laminated on both sides of the substrates

using the roll laminator. The laminated substrates were then exposed and developed to obtain the openings for the bond-pads and the fine line structures. To maximize the resolution during exposure, a hard contact and a high intensity light source were used.

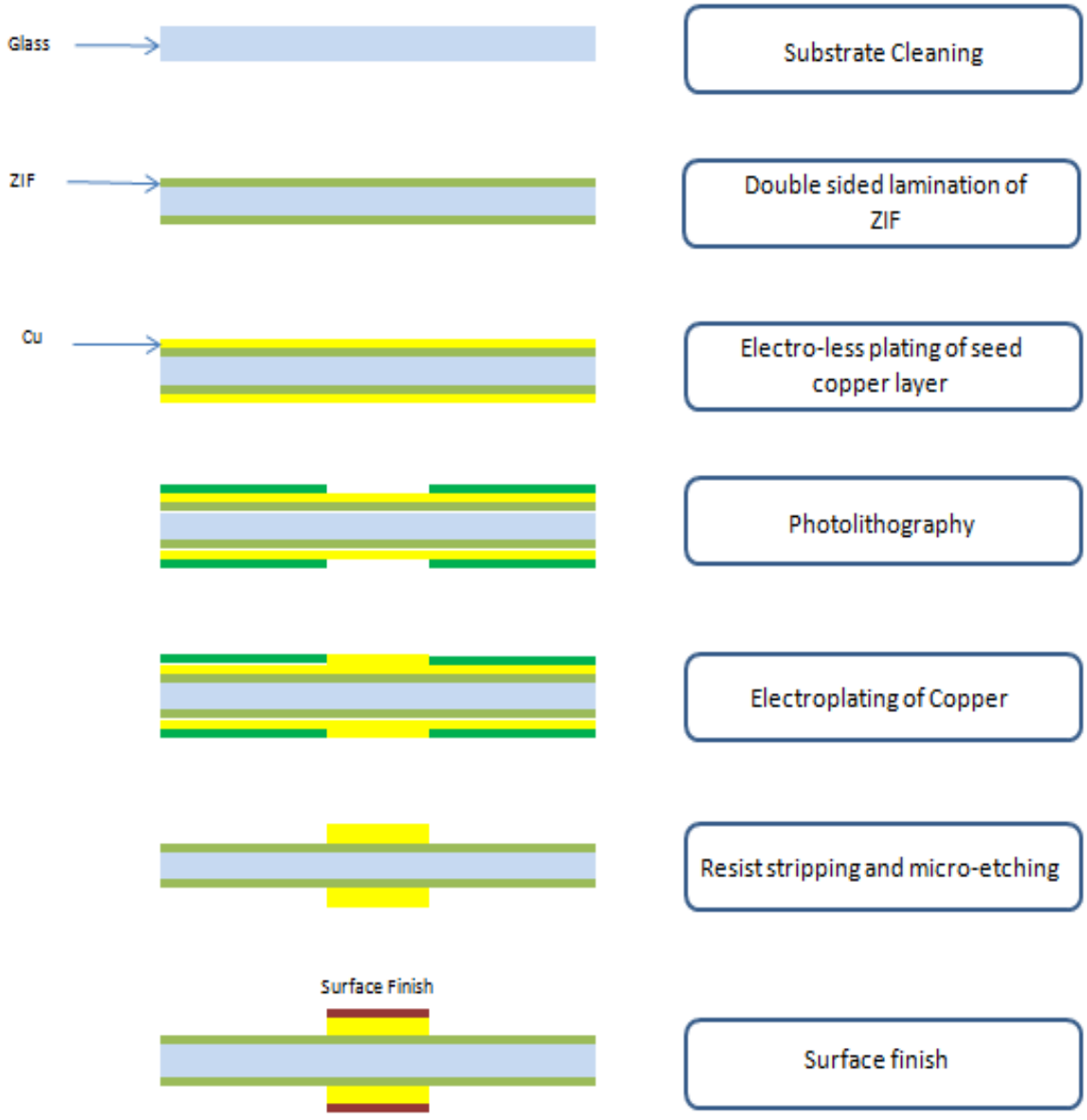


Figure 29: Baseline process for fabrication of glass substrates

Once the substrates were patterned, copper was electroplated using the Cupracid TP chemistry to form the structures on the substrate. 10 microns of copper was plated at a plating rate of 0.33µm/min, using a current density of 15mA/cm^2. After plating, Enthone PC 4025 solution was used to strip the photoresist. After stripping the photoresist, the substrates were immersed in a mild copper etchant for 30 seconds to etch away the seed layer. This was followed by a plasma cleaning step to remove the organic residue.

Electroless Nickel and Immersion Gold (ENIG) surface finish was coated on the traces and bump-pads to prevent oxidation of copper. ENIG is widely used in the industry as a surface finish for printed circuit boards. ENIG has several advantages over conventional surfaces finishes such as excellent surface planarity, good oxidation resistance, superior wettability, and long shelf life.

Table 4.8 shows the steps for the ENIG process, and the bath composition, temperature and plating time for each of the steps. Aurotech chemistry, developed by Atotech, was used for coating the ENIG surface finish. This consists of nickel sulphate based chemistry for the nickel electroplating and gold cyanide chemistry for the immersion gold layer. The thickness of the nickel and gold layers deposited was 5 microns and 0.1 microns respectively. Figure 30 shows images of the substrate post ENIG surface finish.

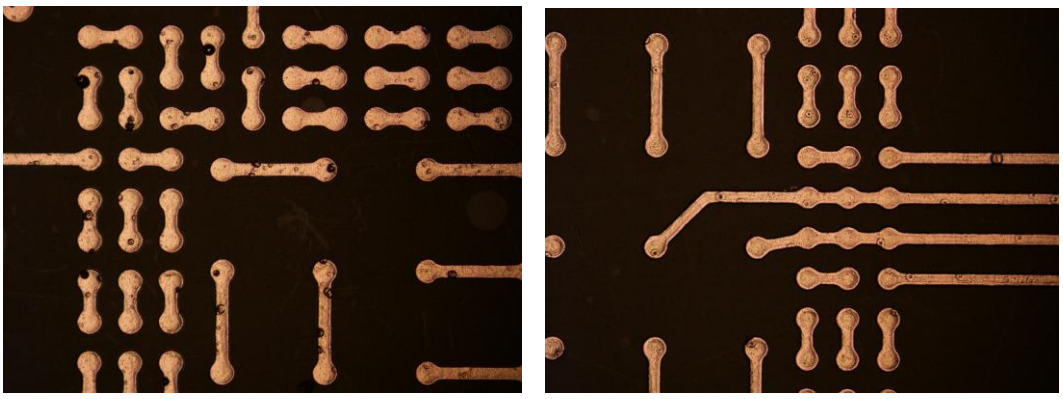


Figure 30: Images of glass substrate with ENIG finish

Table 4.8: ENIG process steps

Oxide cleaning	H_2O	950 mL	RT*	30 s
	H_2SO_4	50 mL		
Pd Poison	H_2O	225 mL	40°C	5 min.
	Proactive DP	250 mL		
	H_2SO_4	25 mL		
Cu cleaning	H_2O	375 mL	45°C	5 min.
	H_2SO_4	33 mL		
	SF Acid	100 mL		
Rinse	Rinse: Water beaker			
	Rinse: Spray			
Oxide cleaning	H_2O	950 mL	RT*	30 s.
	H_2SO_4	50 mL		
Rinse				
Aurodip	H_2O	870 mL	70°C	2 min.
	Aurodip	130 mL		
Rinse				
Predip / Oxide cleaning			RT	1 min.
Activator	H_2O	750 mL	RT	Variable
	H_2SO_4	50 mL		
	Activator	200 mL		
Rinse				
Electroless Ni	H_2O	390 mL	85°C	Variable
	Make up	75 mL		
	Part A	30 mL		
	NH_4OH	10 mL		
Rinse				
Immersion Au	H_2O	700 mL	85°C	Variable
	SF Plus	238 mL		
	SF Starter	1 mL		
	KAuCN	3 g		
	H_2SO_4 / KOH	pH = 4.8		
Rinse	Water beaker + Hot water beaker			

4.4 Assembly Process

Interconnections assembly becomes challenging as the pitch is decreased to small values. Decreasing the pitch also results in scaling down of the interconnect height and solder volume, which makes it harder to overcome non-coplanarity by solder collapse during reflow. Thus, thermo-compression bonding is the preferred assembly technique used for interconnection pitches less than 100 microns. In this study, assembly was performed by thermo-compression bonding using the FINETECH Fineplacer Lambda

assembly tool, which has an alignment accuracy of +/- 0.5 microns. Issues related to die-tilt during placement on the substrates were solved with the help of a tool-head having gimbal capability, which allowed for pre-leveling of the die to ensure parallelism during assembly.

Traditional capillary-flow underfill materials with inorganic fillers that are currently used in flip-chip manufacturing cannot meet the requirements for stand-off height at high throughput. To address these limitations, a novel Namics-proprietary B-Staged No-flow Underfill (BNUF) material and process was used in this research. The underfill was modified with latent curing agents to suppress fasting curing and to make it compatible with lead-free solder reflow process, thus providing a careful control of the solder-spread and bump shape.

The first step was screen-printing a controlled volume of the underfill on the dies, by using a 50 micron thick mask. This was followed by drying it in a N_2 oven at 70^{o}C for 60 minutes. This step, also referred to B-staging of the underfill, was performed in order to evaporate the solvent content from the underfill material. Using the flip-chip bonder, the die was then picked and aligned to the substrate, first roughly based on the corner fiducials plated on both die and substrate, then on the bump to achieve finer placement accuracy.

The bonding was performed at a temperature of 250^{o}C, about 30^{o}C above the solder melting point, as is classically applied in high-volume reflow processes. Ramp rates between 1 and 6^{o}C/sec were used during cool-down to study their effect on the copper-solder bonding. The dwell time at peak temperature was between 3-15 seconds. The applied force for the 5x5 mm^2 die size was 7.5N, which resulted in an equivalent pressure of ~15MPa. For the 10x10 mm^2 die size, the force was determined based on the effective area, so as to maintain the pressure around 15MPa. Other pressures between 6 and 25 MPa were also tested, to study its effect on the copper-solder bonding. Figure 31 shows one of the temperature profiles used for the assembly.

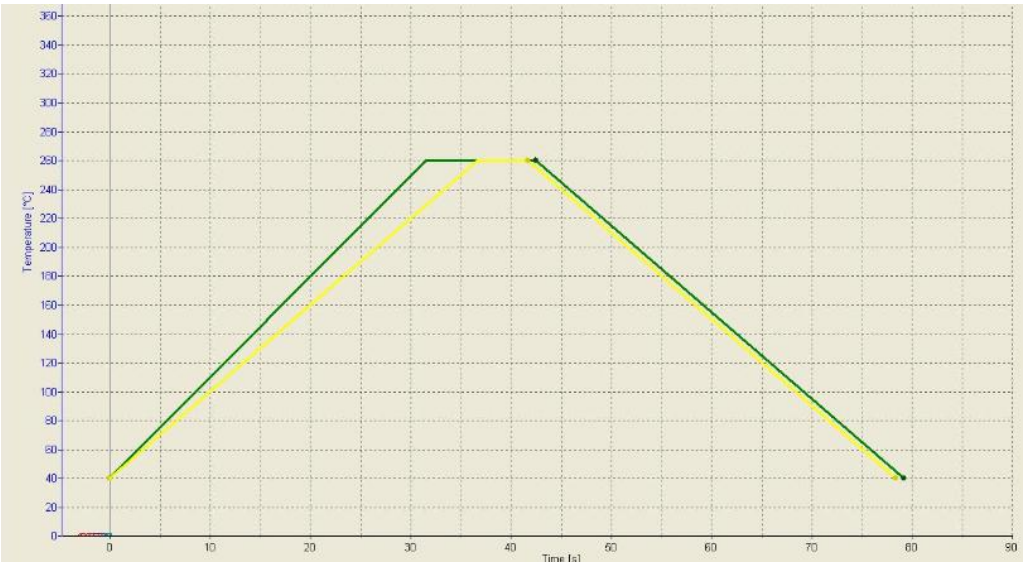


Figure 31: Temperature profile for thermo-compression assembly

The temperatures of the die and substrate during assembly are controlled by the heating modules connected to the heating plate and tool head respectively. The individual temperature profiles for these two are developed so as to ensure minimum temperature gradient. Figure 32 shows the process flow for the die-to-substrate thermo-compression assembly.

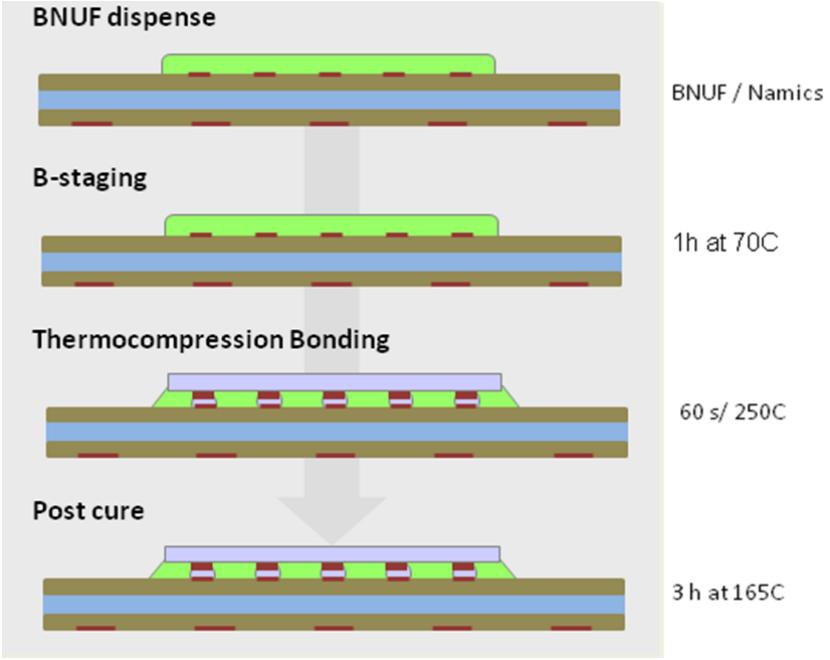


Figure 32: Process flow for die-to-substrate assembly

BNUF becomes liquid at 100-110^{o}C, which allows flow of the excess material under the bonding pressure. At 200^{o}C, it starts curing, and is almost completely cured by the end of the process. However, being a polymer-based material and having a low T_g, it is still soft at this stage. For this reason, the assembled samples were cured at 165^{o}C for 3 hours.

4.5 Characterization Techniques

Interconnections formed using the assembly process mentioned above were characterized to study the effect of bonding parameters such as temperature, pressure and time on the copper-solder bonding. The different characterization techniques used during this study are listed below.

4.5.1 Optical Microscopy

An optical microscope was used for preliminary observation of the assembled interconnections. The samples were initially cold-mounted, after which they were mechanically polished, initially using sandpapers with increasing grit sizes, and finally with polishing cloths. The polished samples were imaged using the optical microscope to study the joint-quality.

4.5.2 Scanning Electron Microscopy

Field Emission Scanning Electron Microscope (FE-SEM LEO 1530) was used for high magnification and high resolution images. SEM imaging was used to study the IMCs formed between copper and tin, which were not observable using the optical microscope.

4.5.3 Energy Dispersive X-Ray Spectroscopy (EDS)

The formation and growth of copper-tin intermetallics was studied using EDS. Point, line and area scans were performed to study the distribution of copper and tin near the bonding interface, and thus determine the composition at different locations of the assembled bumps. This helped in studying the effect of bonding parameters on the copper-tin IMC growth. EDS was also used to study the effect of current density on the composition of electroplated SnAg solder.

4.5.4 3D Microscopy

LEXT 3D confocal microscope was used to study the bump height variation for the electroplated Cu-SnAg interconnection bumps. Bump height was measured at various locations within a die, and for dies at various locations across a wafer, in order to study the effects of die and wafer design on the plating rate for electroplating.

CHAPTER 5

RESULTS AND DISCUSSIONS

The first part of this chapter describes the optimization and characterization of the bumping process for fine-pitch ultra-short copper-solder interconnections. This is followed by the assembly characterization of these interconnections, and a study on the effect of bonding parameters on the copper-solder bonding is presented. The final part of the chapter focuses on the development of the copper-solder stacked interconnections technology.

5.1 Bumping Process Development for Ultra-short Copper-Solder Interconnections

Following the fabrication procedures described in Chapter 4, fine-pitch copper-solder bumps were fabricated on 4" and 6" wafers with test vehicle designs A and B. The interconnection bump structure was made up of 5 microns copper and 10 microns SnAg solder, leading to a total bump height of 15 microns. The critical steps in the wafer fabrication process were copper and solder plating. Plating process parameters have an effect on three major characteristics of the electro-deposited bumps, namely composition, height and morphology. The effect of plating parameters on each of these characteristics was studied in detail.

5.1.1 Solder Composition Control

Having a control over the composition of the deposit is important because it determines the melting point of the solder. By keeping the Ag content close to 3.5 atomic %, which is the eutectic composition (Sn-3.5%Ag), the solder can be reflowed at the minimum temperature possible (221^0C). Slight changes in the Ag content can lead to a considerable change in the melting temperature of the solder. Thus, controlling the Ag content of the deposit is critical while plating using SnAg co-alloy.

With co-plated SnAg alloys, deposition of tin-rich alloys is difficult due to the large difference in the standard reduction potentials of Sn and Ag, the latter having a higher reduction potential. Moreover, the Ag ions in the electrolyte exist in the monovalent state compared to the divalent or trivalent Sn. Thus, the current required to reduce the Sn ions is two or four times that required for Ag ions [31]. In order to enable deposits to contain high amounts of Sn (>50% by weight), the Ag concentration in the plating solution is kept low. As a result of its low concentration in the solution, Ag deposition from the SnAg co-alloy is a mass transfer limited reaction. Thus, current density has a very small effect on the amount of Ag deposited using these solutions. Deposited amount of Sn, on the other hand, increases with current density. This leads to decreasing silver content in the electro-deposit with increasing current densities.

Experiments were carried out to obtain the targeted eutectic composition of SnAg by varying the current density of electroplating. SnAg solder, at varying current densities, was electro-deposited on 3 x 3 inch silicon samples coated with a few microns of copper. The composition of these SnAg films was analyzed by energy dispersive X-ray spectrometry (EDS) and X-ray photoelectron spectroscopy (XPS). Figure 33 shows the plot representing this experimental data, with the Ag content plotted against the current density. A regression line was drawn along with error bars for the silver content measurements. It was found that the Ag composition in the electrodeposit decreased from the near-eutectic 3.59 to 1.21 atomic percent as the current density was increased from 15 to 25 mA/cm^2. A current density value of 15mA/sq.cm was determined to be the ideal current density for deposition of eutectic composition of SnAg for this particular plating solution.

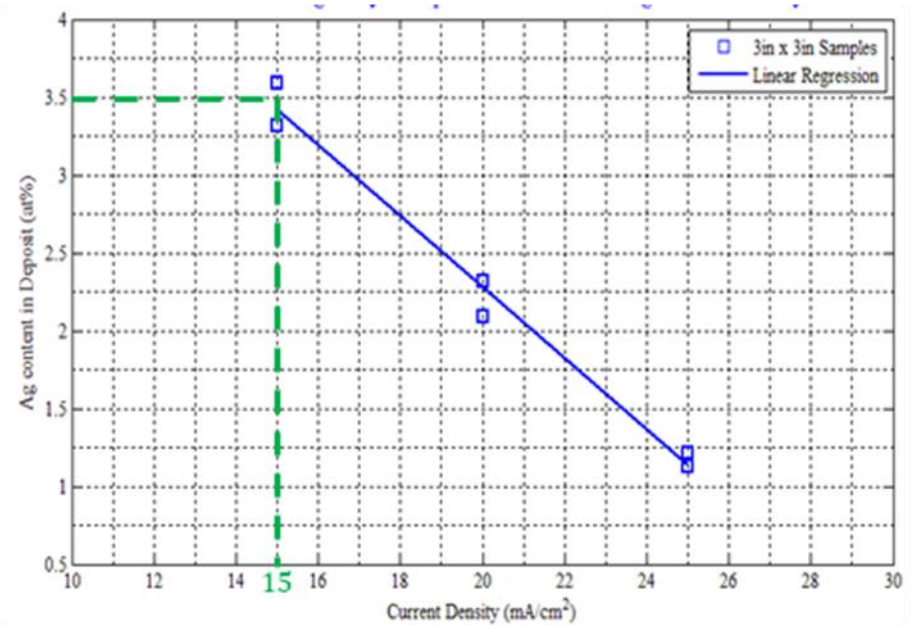


Figure 33: Effect of varying current density on the electro-deposited silver content

5.1.2 Bump Height Analysis

Interconnection bumps were fabricated by electroplating copper and SnAg solder, as discussed in Chapter 4. The height of the bumps at any location in the wafer is a function of the local plating rate. Several critical factors affect the local plating rate such as metal concentration in the bath, plating bath configuration and design, current densities, bath additives, levelers, edge effects and shielding. These factors lead to a variation in the local current density at different locations on the wafer, thus affecting the local plating rate.

Of more importance to wafer fabrication is the role played by the active area density on the local current density [32]. The active area density represents the change in the electro-active area of the wafer due to lithographic patterning of the wafer. Patterning leads to variations in the active area density within a die as well as at different location across a wafer.

Using the test vehicle B, described in Chapter 4, plating height analysis was performed to study the variation within a die and across the wafer. 3D microscopy was used to measure the bump heights. Dies were selected at random from a 4 inch wafer, 5 from the center of the wafer and 5 from the wafer edge. Within each die, the bump height was measured at different locations for the peripheral and area-array bumps, and then averaged for each for that die. Table 5.1 shows the tabulated results for this exercise.

Table 5.1: Bump height variation for (a) dies at wafer edge and (b) dies at wafer center

Die	Avg. Peripheral Bump Height (um)	Avg. Central Bump Height (um)
1	14.9	15
2	16.2	15.5
3	15.2	16.5
4	15.1	15.8
5	16.5	16.6
Avg.	15.6	15.9

(a)

Die	Avg. Peripheral Bump Height (um)	Avg. Central Bump Height (um)
1	11.7	13.1
2	12.5	14.2
3	14.1	13
4	9.2	9.5
5	13.8	14.1
Avg.	12.3	12.8

(b)

5.1.2.1 Variation Across a Wafer

While designing a wafer, usually a ring of exposed metal is left at the periphery of the wafer to assist in providing electrical contact during electroplating of copper and solder, as shown in Figure 34. This ring of exposed metal, usually 0.5-1 cm in width, critically affects the active area density for dies closer to the wafer edge, leading to higher active area densities at these locations. An increased active area density means a lower local current density, as the same amount of current is directed at all areas across the wafer. The lower active current density for dies at the wafer edge corresponds to a lower plating rate for bumps located in these dies. As the plating time is a constant, a lower plating rate further corresponds to a lower bump height. Thus, the dies at wafer edges have bumps with lower height as compared to dies at the wafer center, which is also observed from Table 5.1.

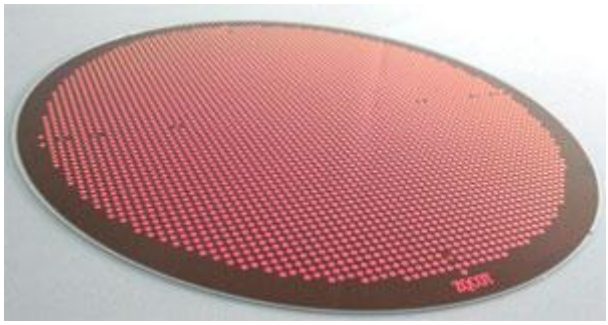


Figure 34: Patterned wafer with exposed metal ring at the periphery

5.1.2.2 Variation Within a Die

In a die, the signal bumps are usually located at the die periphery and the ground bumps at the die center. The peripheral bumps are commonly designed at a finer pitch than the coarse area-array bumps at the die center. This leads to a lower active area density at the central region as compared to the die periphery. Active current density is higher in areas where the active area density is lower i.e. centre of the die. Higher active current density leads to a higher plating rate for central bumps. Accordingly, bumps in

the central region have a slightly higher bump height than peripheral bumps. This is also reflected in the results in Table 5.1 above.

5.1.3 Effect of Current Density on the Surface Morphology

The morphology of the electroplated SnAg is affected by the current density used for plating. An increase in the current density leads to an increase in the cathodic overpotential on the electrodeposit. The increased cathodic overpotential leads to a higher nucleation rate, causing the microstructure to be finer and smoother with increasing current densities [33]. SnAg was electroplated on silicon wafers having pre-plated copper layer of 5 microns. Samples were prepared with varying current densities of 5, 10, 15 and 20 mA/cm^2, and the microstructures were studied using the SEM. Figure 35 shows the microstructural images for samples with increasing current density. It is seen that the microstructure becomes finer with increasing current density.

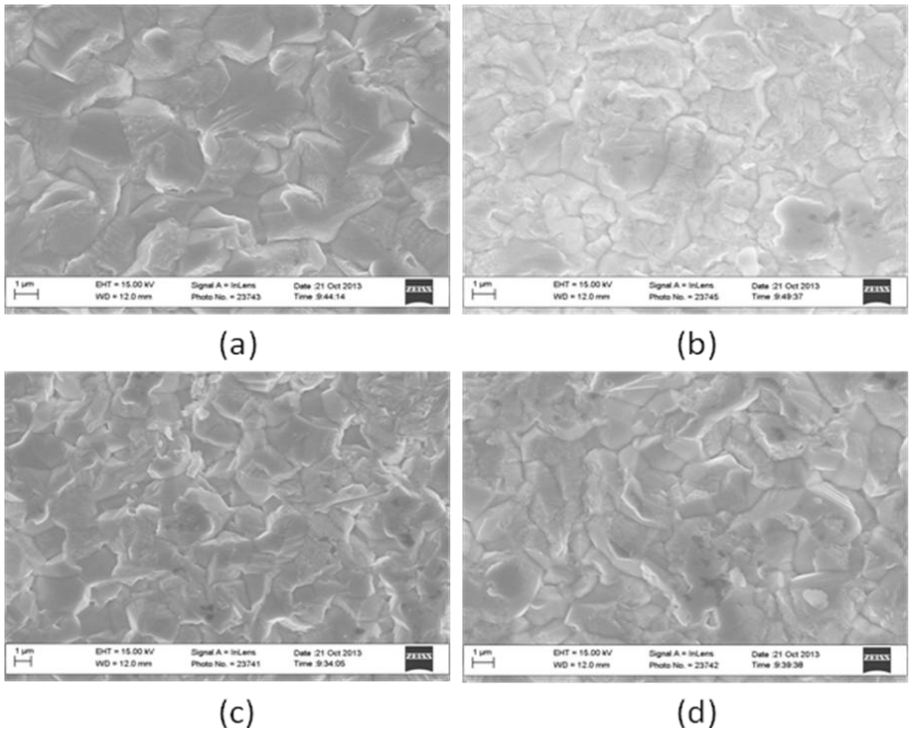


Figure 35: Microstructural images with increasing current densities (a) 5mA/cm^2 (b) 10mA/cm^2 (c) 15mA/cm^2 (d) 20mA/cm^2

5.2 Assembly Process Characterization and Optimization for Ultra-short Fine-pitch Copper-Solder Interconnections

Using the finite element modeling results obtained in Chapter 3 as design guidelines, 50 and 100 micron pitch interconnections were fabricated with a stand-off height of 15 microns. The dies were assembled onto glass substrates, which were fabricated using the process flow described in the previous chapter. A FINETECH Fineplacer Lambda with a placement accuracy of +/- 0.5 micron was used to achieve die-to-substrate assembly by thermocompression bonding at 250^{o}C. Preliminary trials were performed with a dwell time at peak temperature of 10 seconds for a total process time of about 80 seconds and 7.5N of applied force, equivalent to a 15 MPa pressure.

Cross-sections of initial assembled samples showed only partial landing of the bumps on the substrate pads. This poor yield was attributed to die-tilting introduced by the standard flat pick-and-place tool-head used for assembly. Figure 36 displays overlapping images taken from left to right along the cross-section, where the die tilt and its effect on the interconnection yield can be clearly observed.

Figure 36: Overlapping images showing the effect of die-tilt on interconnection yield

To prevent any die tilting during assembly, which is extremely penalizing in thermocompression bonding, a novel gimbal tool-head was introduced. The head of this specific placement tool is attached to a spring, allowing pre-leveling of the head by gimbaling on the die backside when picking it up. The gimbal can then be vacuum-

locked to ensure parallelism of die and substrate during bonding. Assembly with a 100% interconnection yield can be achieved with this gimbal tool, even for a large die with high I/O density (design A) as confirmed by Figure 37 showing a substrate after die shear test with proper wetting of solder on all landing pads across the die.

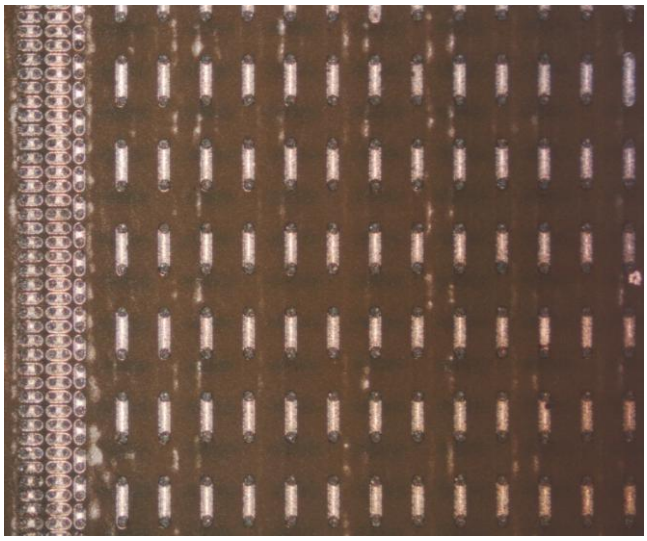


Figure 37: 50 micron pitch substrate post die-shear test

Preliminary trials with the gimbal tool highlighted a more concerning issue: even though all bumps are landed on the copper traces, the majority of them featured cracks right after assembly as displayed in the picture of Figure 38. This failure mode was extensively investigated to gain an understanding of the fundamental mechanism behind crack initiation and explore solutions to counter it.

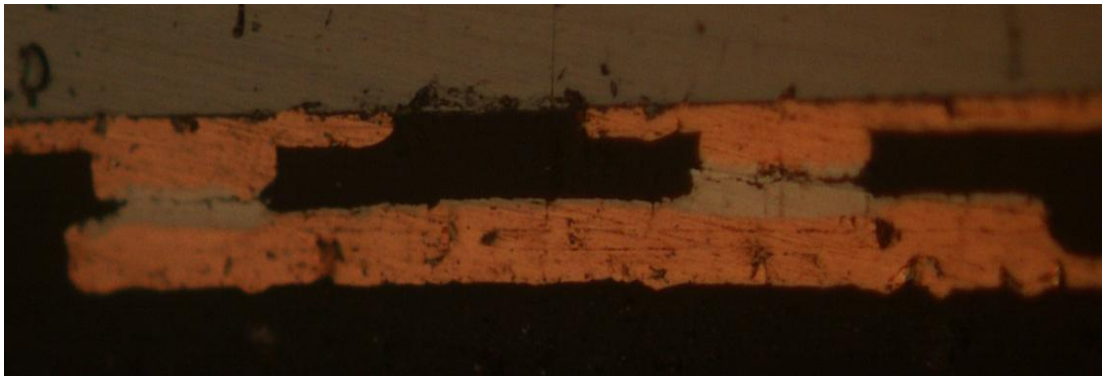


Figure 38: Joint-cracking observed post assembly with ultra-short copper-solder interconnections

5.2.1 Determination of Location of Joint-Cracking

In order to understand the mechanism behind the observed joint-cracking, it was important to determine the location at which these cracks were being generated. Preliminary observations of the joint cross-sections using optical microscopy showed the presence of cracks in the solder, closer to the die-side. However, the exact location was not determinable using optical microscopy, since the magnification was not high enough. For this reason, the LEO 1530 SEM was used to observe the cross-sections of the assembled joints.

Finite-element modeling results have shown that increasing IMC thickness results in an increase in the post-assembly stresses developed in the interconnection bumps. To understand better how the IMCs affect the cracking, EDS was performed to locate the IMCs present in the assembled joints. Point scans were performed at various locations along the normal to the copper-solder interface, to determine the location of the IMCs with respect to the cracks. Figure 39 displays an SEM image of the assembled joint showing locations of various scans performed on its cross-section, and Table 5.2 lists the metal, alloy or compound present at each location based on the composition of elements detected through EDS.

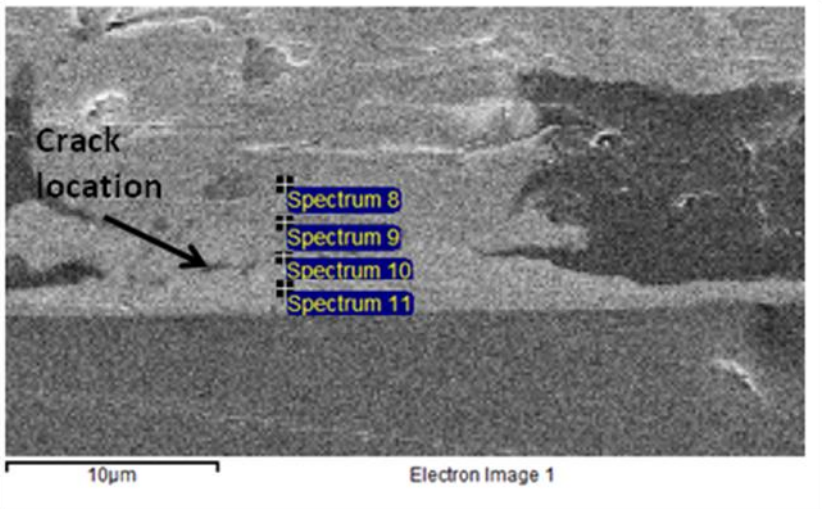


Figure 39: SEM image of joint cross-section showing locations of point scans

Table5.2: Results of EDS point scans

LOCATION	MATERIAL
Spectrum 8	Cu
Spectrum 9	Cu_3Sn
Spectrum 10	Cu_6Sn_5
Spectrum 11	$Sn_{3.5}Ag$

It can be seen from Figure 39 that the crack is located between the locations of the point scans for spectrums 10 and 11. This corresponds to the crack being present at the solder-IMC interface, or more specifically between the SnAg solder and Cu_6Sn_5 intermetallic. This result is also supported by finite-element analysis, which showed the concentration of stress in the joints at the solder-IMC interface.

5.2.2 Origin of Post-Assembly Joint-Cracking

Stress concentration in solder joints can arise from material-induced mechanisms such as mismatched thermal expansion or warpage of the structure, or from non-optimized process parameters such as underfill curing profile, bonding temperature, time, or pressure. Any or all of the listed characteristics could potentially be responsible for the joint-cracking observed post assembly. To analyze the cause for crack initiation, effects of several factors on the bonded joints were studied.

5.2.2.1 Effect of Substrate Warpage

Glass has a CTE of 3.8ppm/^{o}C, which is slightly higher than the CTE of silicon, which is 3ppm/^{o}C. During the cooling-down phase of thermo-compression assembly, the substrate contracts more than the die, thus bending into a slightly convex shape, as shown in Figure 40. Substrate warpage may also result due to materials stack-up, geometry,

stiffness and thickness. This substrate warpage exerts stresses on the bonded joints. If this warpage is significantly high, it could lead to joint-cracking induced by shear stress.

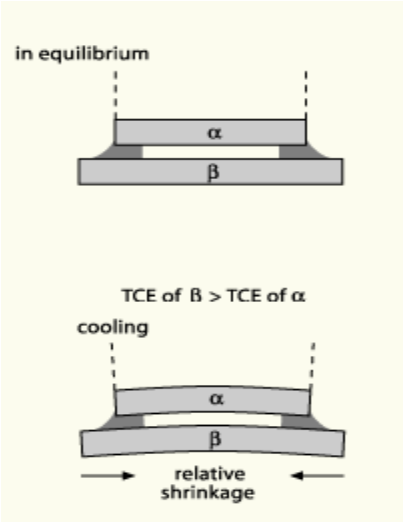


Figure 40: Substrate warpage due to CTE mismatch between die and substrate

Thick silicon substrates were used as control samples to determine if the joint-cracking was a result of substrate warpage. Along with eliminating the die-to-substrate CTE mismatch, the thick silicon also resists deformation due to its high stiffness. Figure 41 shows the cross-section images for interconnections formed by silicon die-to-silicon substrate assembly. Joint-cracking was observed even with this control sample, leading to the conclusion that warpage was not responsible for it.

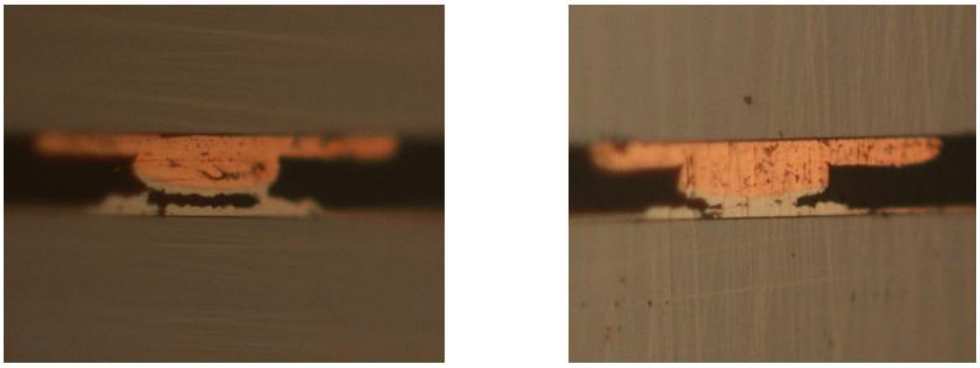


Figure 41: Joint cross-sections using thick silicon substrates as control samples

5.2.2.2 Effect of Underfill Viscosity and Curing Profile

In the case of pre-applied underfills, viscosity and curing profile of the underfill have an effect on the stress state in the joints after assembly, as described below. Viscosities for most pre-applied underfills follow the curing profile shown in Figure 42, where the viscosity initially decreases with temperature, reaches a minimum value, and then increases with temperature and time until the underfill is cured.

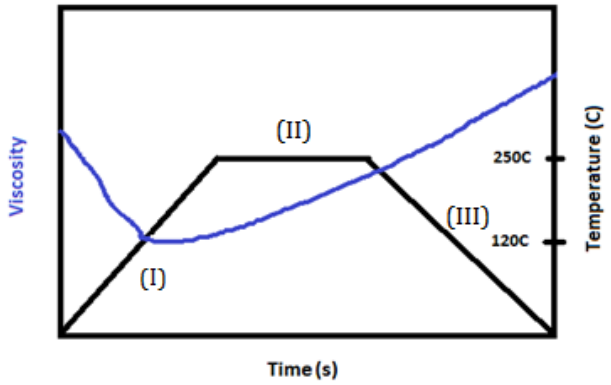


Figure 42: Generic curing profile of pre-applied underfills

During phase (I) of bonding, the viscosity of the underfill decreases and reaches its minimum value. This decreased viscosity allows the copper-solder bumps to penetrate into the underfill and land on the substrate. During phase (II), the solder melts and gets bonded to the copper pads on the substrate. Simultaneously, polymer cross-linking occurs in the underfill and its viscosity increases. If the underfill hardens too quickly, it results in a fixed stand-off height between the die and substrate. In the molten state, the solder fills the volume between the die and substrate, which is not occupied by the hardened underfill. However, the solder and the intermetallics contract during phase (III) of the bonding, resulting in tensile stresses being generated in the solder as a result of the fixed stand-off height.

To determine whether interconnect failures were caused by inappropriate curing conditions for the BNUF material used in this study, assembly trials were performed with

flux and post-applied capillary underfill. Figure 43 shows the joint cross-section for a sample assembled using this process flow. Cracks were present even in this case, thus confirming that the failure mode is not related to the chosen underfill material.

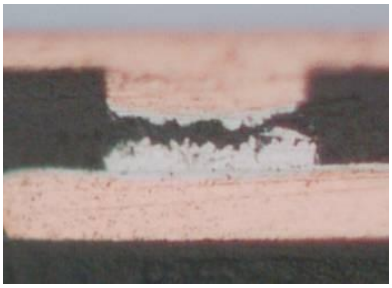


Figure 43: Joint cross-section for interconnections assembled using post-applied capillary underfill

5.2.2.3 Effect of Bonding Pressure

Bonding pressure affects the amount of solder-squeezing and solder-spreading that occurs during assembly. Squeezing of solder due to high pressure leads to a decrease in the solder height. Lower solder height and high solder-spreading have both been shown to have adverse effects on the stresses developed at the solder-IMC interface post assembly, as predicted by finite-element modeling experiments performed in Chapter 3. To study the role of pressure on the joint-cracking, samples were assembled with varying loads of 7.5, 10 and 12.5N which resulted in equivalent pressures of 15, 20 and 25MPa. However, no significant change in solder-squeezing, solder-spreading or joint-cracking was observed, as can be seen in Figure 44.

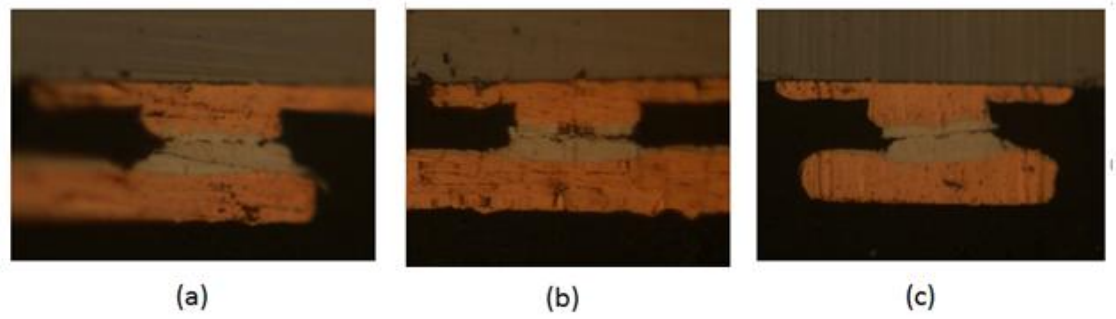


Figure 44: Effect of varying bonding pressures on joint-cracking behavior (a) 15Mpa (b) 20Mpa (c) 25Mpa

5.2.2.4 Effect of Solder Volume

To study the effect of solder volume on joint-cracking, interconnection bumps were fabricated with solder heights of 5, 7 and 10 microns, plated on top of 5 micron tall copper-pillars. These were then bonded to glass substrates using the assembly process previously described. Figure 45 shows the cross-sectional images for these interconnections, captured using an optical microscope. Although joint-cracking was observed in all the three cases, the crack length varied with solder height. Interconnections with higher solder height only presented signs of crack initiation, while the shorter bumps were fully cracked. This result also reiterated the adverse effects of decreased solder heights on the stresses developed in solder joints, as was observed through finite-element modeling.

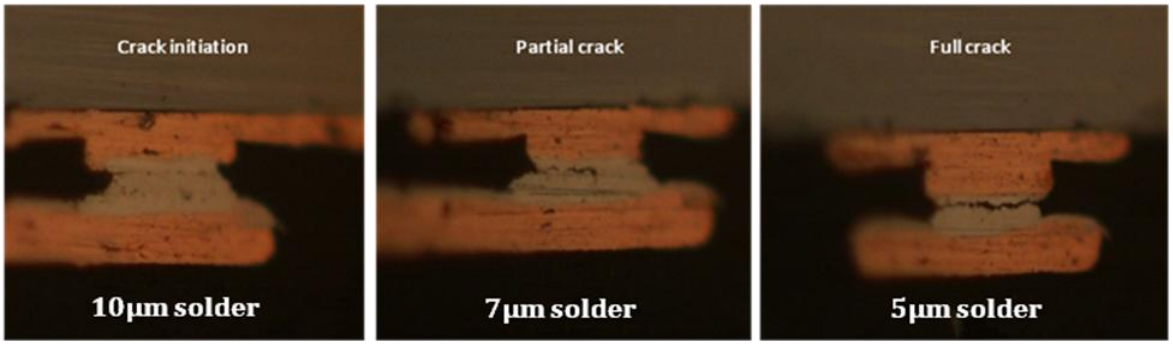


Figure 45: Variation in crack length with solder height

5.2.3 Mechanism for Joint-Cracking

SnAg solder and the copper-tin intermetallics formed during assembly significantly differ in their mechanical properties, leading to development of stresses in the interconnection bumps during the cooling down of solder. These stresses are concentrated at the interface between the solder and the intermetallics, which was verified both by finite-element modeling and also indicated by the presence of cracks at the solder joints. Solder being the more ductile material of the two, has the ability to

accommodate the stresses developed as a result of mismatch of mechanical properties. As the interconnection stand-off height decreases, solder volume thus becomes critical.

For interconnection bumps having high solder volumes, the solder dominates the mechanical properties of the bumps. However, decreased solder volume results in increased stresses, arising from the mismatch in the mechanical strengths of solder and IMCs, which are now present in comparable amounts. Moreover, the reduced solder volume is not able to accommodate all of the stresses that are developed. This may ultimately leads to cracking in these bumps at the solder-IMC interface, as was observed in this study.

5.2.4 Considerations for Prevention of Joint-Cracking

It was found that joint-cracking in ultra-short copper-solder interconnections resulted from decreased solder volumes, which were not able to accommodate the stresses developed at the solder-IMC interfaces. This has an adverse effect on the interconnection reliability, and this issue needs to be addressed in order to achieve good-quality joints at fine pitches and low stand-off heights. Based on the finite-element modeling results from Chapter 3, the factors that can help in decreasing the stress at the solder-IMC interface are high solder volume, limited solder spreading, low IMC thickness and slower solder cooling rate during bonding. For interconnections with low stand-off heights, it is not possible to increase the solder volume any further. A slower cooling rate for the solder during assembly was found to have only a small effect on the stress (<10%). This leaves two key knobs to control the stress, IMC thickness and solder spreading.

As previously stated, IMC formation is a diffusion-driven process. As such, the rate of formation of IMCs is enhanced at higher temperatures. Reducing the time spent over the melting point can help decrease the IMC thickness, and thus result in decreased stresses at the solder-IMC interface. FEM also showed that lower cooling rates leads to

decreased stresses. Thus, the bonding profile needs to be optimized to reduce the dwell time while keeping the cooling rate low. Another method to control the IMC thickness is by introducing a barrier layer such as nickel, between the copper and solder. The rate of dissolution of nickel in copper is significantly lower than the rate of dissolution of tin in copper. As a result, 1-2 microns layer of nickel helps to reduce the IMC thickness.

Several measures can also be taken to control the spreading of solder on the substrate. The conventional approach to control solder spreading involves the use of passivation layers on the substrate that help to maintain the bump shape. However, building a passivation layer is increasingly difficult at finer pitches, and also increases the number of processing steps, thus decreasing the throughput for these interconnections. Solder-spreading and bump shape can be controlled effectively by controlling the viscosity and curing profile of the underfill. Another approach, which was used by Paik et. al. while demonstrating 40 micron pitch copper-solder interconnections with 20 microns stand-off height, involves low bonding pressures and removal of the pressure once the bumps are in contact with the substrate pads [18].

Yet another alternative to eliminate the stresses at the solder-IMC interface involves eliminating the solder-IMC interface itself. This can be done by converting all of the solder to IMCs, so as to have uniform composition across the joint. SLID bonding has been previously used to completely convert the solder to stable intermetallics. This approach not only addresses the joint-cracking issue, but intermetallics have also been shown to be more electromigration-resistant than solders, thus improving reliability at high current-densities.

5.2.5 Ultra-short Crack-Free Joints

Based on modeling and fabrication results, critical factors affecting joint-cracking were identified and optimized. Interconnection bumps with 10 microns solder height, as determined by modeling, were fabricated to better accommodate the internal stresses. A

reduced pressure of 1.5Mpa was used to assemble the interconnections, which resulted in minimized solder spreading. The dwell time used for the assembly process was decreased to 5 seconds to reduce the thickness of the formed intermetallics. By optimizing the bumping and assembly process using these parameters, crack-free joints were achieved for assembly with glass interposer, as shown in Figure 46.

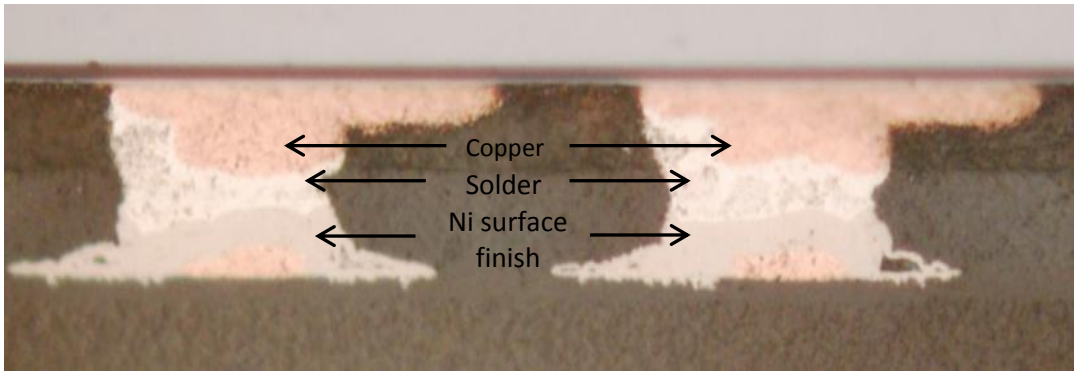


Figure 46: Cross section image of ultra-short crack-free joints

5.3 Ultra-short Fine-Pitch Copper-Solder Stacked Interconnections

One of the major challenges to conventional copper-solder interconnection approaches, when scaled down to fine pitches and low stand-offs, arises from the co-presence of intermetallics and residual solder in the joints post-reflow. Irrespective of the decreased solder volume with decreased stand-off, the thickness of the IMC layer stays constant. Thus, as interconnections become shorter, the IMCs become more prominent and dominate the thermodynamical behavior of the joints [34]. Thus, SLID bonding approach was explored for ultra-short interconnections, where the solder is completely converted to stable intermetallics. A new copper-solder stacked interconnections approach was proposed earlier to overcome the challenges of ultra-short interconnections at fine pitches.

5.3.1 Fabrication of Copper-Tin Multi-layer Stack

As proof of concept, 100 micron pitch interconnections with multi-layer copper-tin stack were fabricated using the test vehicle B, described in Chapter 4. The process was completed in two photo-lithography steps, one for the routing layer and the other for the bumps.

The procedure to fabricate the routing layer was similar to the fabrication process described in Chapter 4. Hitachi RY-5315EB dry-film photoresist having a thickness of 15 microns was used for patterning the routing layer. Karl-Suss MA6 Mask Aligner was used to expose the wafers with a dose of 95mJ/cm^2 using hard contact, after which they were developed in 3% Na_2CO_3 solution at 85^{o}C for about 2 minutes. Once the photoresist development was complete, the wafers were plasma-cleaned to remove organic residue, if any, from the openings in the photoresist. Copper was then electroplated through these openings to form a 2-3 microns thick routing layer. Finally, Enthone PC 4025 was used to strip the photoresist.

The same 15 microns thick photoresist was used for patterning the bumping layer. Photoresist lamination, exposure and development steps were similar to the ones followed for patterning the routing layer. After patterning, the wafers were plasma-cleaned, before continuing with the plating process. Copper and tin were plated alternately to obtain the copper-tin stack structure. Cupracid TP chemistry was used for plating copper while tin was plated using the Stannobond FC chemistry, both provided by Atotech. The wafers were thoroughly rinsed and dried after electroplating each layer of the bump, so as not to contaminate the two plating baths. The current densities used for copper and tin electroplating were 15mA/cm^2 and 20mA/cm^2 respectively, and the resultant plating rates were 0.33μm/min and 1 μm/min respectively. The plating time for each layer was determined based on their respective target thicknesses. The plated thickness was measured after each plating step using the Dektak Profilometer.

Once the plating was completed, the photoresist was removed using the Enthone PC 4025 stripper solution. This was followed by seed layer etching to remove the underlying copper and tin seed layers. A blanket wafer was used to demonstrate the copper-solder multi-layer stacked structure. The alternate layers of copper and tin are clearly visible, as can be seen in Figure 47.

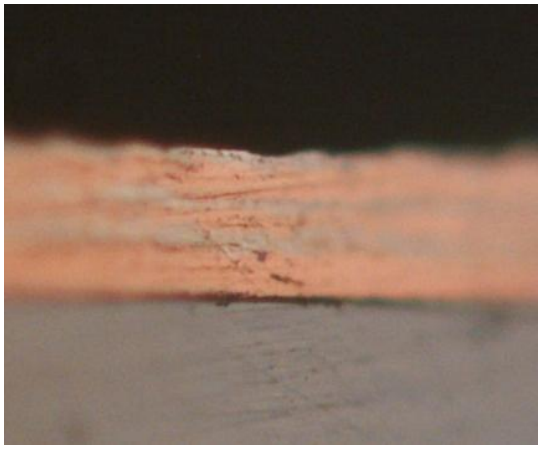


Figure 47: Copper-solder multi-layer stacked structure deposited on blanket wafer

The wafers were finally diced into individual dies, which could then be assembled. The substrates used for assembling these dies were similar to the ones fabricated for the copper-pillar and solder-cap interconnections, as described previously in Chapter 4.

5.3.2 SLID Bonding Assembly with Copper-Solder Stacked Interconnections

The fabricated multi-layer copper-tin stacked interconnections were assembled using SLID bonding. SLID bonding assembly ideally has to be performed at a temperature above the melting point of tin, so as to enhance the formation of intermetallics through liquid-state diffusion. In this study, the aim was to convert the tin to the stable intermetallic, Cu_3Sn during the assembly process itself. The stacking of alternate thin layers of copper and tin assisted in completing the Cu_3Sn formation in a much shorter time.

A FINETECH Lambda flip-chip bonder was used to perform for assembly. Pre-applied BNUF was used to improve the reliability of these interconnections. As determined by the diffusion modeling described previously, the bonding temperature and dwell time used were 250^{o}C and 300 seconds respectively. Figure 48 shows the temperature profile used for this assembly process. The force applied during bonding was 7.5N, which resulted in an equivalent pressure of 15MPa.

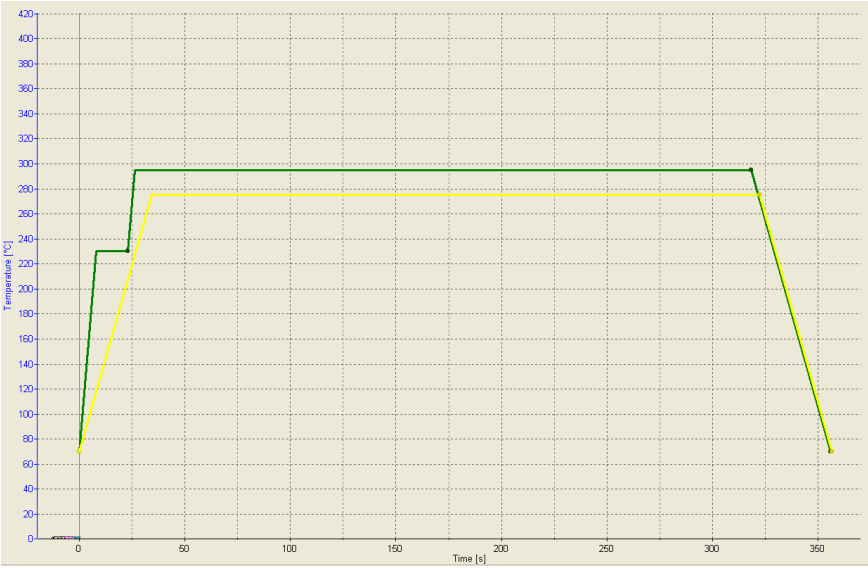


Figure 48: Temperature profile used for SLID bonding of copper-solder stacked interconnections

Initially SLID assembly was performed using interconnections with the traditional copper-pillar and solder-cap approach to validate the formation of Cu_3Sn, as predicted using diffusion modeling. These assembled samples were cross-sectioned and studied using EDS to determine the presence of Cu_3Sn, and its thickness. Figure 49 shows an SEM image of the assembled interconnection. Table 5.3 shows the EDS results for a scan performed at the copper-solder interface of the bonded joint. These are discussed in detail next.

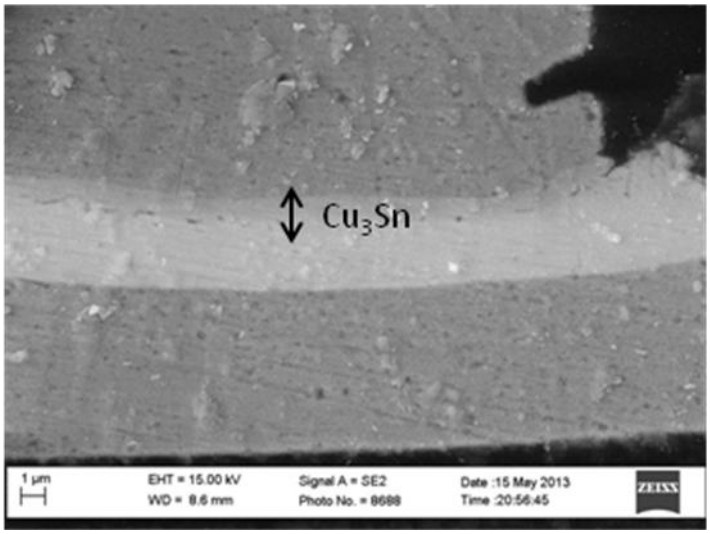


Figure 49: SEM image of SLID bonded copper-solder joint

Table 5.3: EDS result for a scan performed at the copper-solder interface of a SLID bonded joint

Element	App Conc.	Intensity Corrn.	Weight %	Weight % Sigma	Atomic %
Cu K	3.75	1.0448	61.96	0.97	75.26
Sn L	1.98	0.8965	38.04	0.97	24.74
Totals			100.00		

From the atomic percent of copper and tin, it can be inferred that the compound present is Cu_3Sn. To measure the thickness of Cu_3Sn formed at 250^{o}C in 300 seconds, a set of point scans was performed along a line normal to the copper-solder interface, to determine the composition at each point. Based on these scans, the thickness of Cu_3Sn formed was determined to be around 1-1.5 microns. This helped to validate the diffusion model previously presented.

CHAPTER 6

SUMMARY AND FUTURE WORK

The first part of this chapter summarizes the research conducted to explore ultra-short fine-pitch copper-solder interconnections. Recommendations for future work related to this research are provided in the second part of the chapter.

6.1 Summary

Electronic system miniaturization combined with dramatic enhancements in functional density and performance has been primarily driven by increasing transistor densities or Moore's law. This has led to increasing off-chip I/Os or reduced interconnection pitch. The interconnection technology has continuously evolved over the past few decades to meet this need, starting from wire bonding to flip-chip solder bump, and more recently, copper pillar interconnections with solder cap for pitches upto 50-80 microns. To advance the I/O density and reduce the pitch further to 30 microns and below, this research explores two novel copper-solder stacked interconnection technologies, based on ultra-thin solder caps, and combining SLID bonding with a novel multi-layered copper-solder stack, to achieve ultra-short fine-pitch interconnections for high throughput conversion of the entire solder volume to stable and highly-electromigration resistant intermetallics.

FEM was used to study the effect of various assembly and bump-design characteristics on the post-assembly stress distribution in the bumps, for copper-solder interconnections with low stand-off heights. Modeling suggests that the assembly with copper-solder interconnections leads to development of stress-concentration at the solder-IMC interface in the joints during the cooling process. This interfacial stress was found to increase with low solder volume, high solder-spreading on the substrate, high IMC

thickness and faster cooling rate during the bonding process. Based on the modeling, the design guidelines for ultra-short copper-solder interconnections are evolved.

A novel multi-layered copper-solder stack was designed based on diffusion modeling to optimize the bump stack configuration for high-throughput conversion to stable Cu_3Sn intermetallic. The diffusion models predict that a tin and copper layer sequence of 1.5 and 2 microns was required to completely convert the stack into the stable Cu_3Sn phase in less than 5 minutes.

Test vehicles with 50 microns (TV A) and 100 microns (TV B) interconnection pitches and 15 microns bump-heights were designed and fabricated. The dies had bumps 15 and 30 microns diameter for test vehicle A, and 30 and 50 microns in diameter for test vehicle B. Substrates were fabricated from glass, due to its low dielectric constant, low CTE, high dimensional stability and low cost of manufacturing large panels. The dies and substrates were fabricated using a semi-additive process.

The plating process was characterized to study the effect of plating parameters on the solder composition, morphology and interconnection height. Variation of silver content with current density in the electro-deposited solder was observed. Based on those observations, an optimum current density value of $15mA/cm^2$ was determined for deposition of near-eutectic SnAg solder. Variation in bump heights was observed due to variation in the active area densities across the wafer. Dies at the wafer center were observed to have larger bump heights than those located near the wafer edge. Within a die, central bumps were observed to have larger bump heights as compared to the peripheral bumps. The current density seemed to have an effect on the morphology of the electroplated solder, with lower current density values resulting in a finer and smoother microstructure.

The samples were assembled using thermo-compression bonding at 250^oC assisted by a B-stageable no-flow underfill (BNUF). Assembly process characterization

was performed for ultra-short fine-pitch interconnections. Two prevailing issues were faced in assembly: partial landing of the die on the substrate due to die-tilt, and joint cracking during assembly. While the die-tilt issue was solved using a gimbal tool-head, extensive assessment of the effect of various material and process parameters was required to determine the failure mechanism initiating the solder-cracking. The effect of solder volume, viscosity and curing profile of the underfill, substrate warpage and bonding pressure on the joint-cracking was studied. SEM and EDS analysis determined the location of the joint-cracking to be at the solder-IMC interface, similar to the stress-concentration point highlighted in the FEM results. The failures were attributed to the large stresses resulting at the solder-IMC interface due to low solder volume. Based on the design guidelines and assembly process optimization to achieve the targeted design structure, crack-free joints were demonstrated on ultrathin glass interposers.

For the copper-solder stacked interconnections, a novel bumping process with alternating copper and tin plating layers to predesigned thicknesses was developed to fabricate the interconnection structure. Alternate layers of copper and tin were electroplated on a blanket wafer as a first demonstration of this stack-technology. Formation of the stable intermetallic Cu_3Sn was validated by SLID-bonding dies with copper-solder test structures. This novel copper-solder stacked approach can help achieve ultra-short fine-pitch interconnections capable of handling current densities of 10^5 or higher.

6.2 Recommendations for Future Work

A novel approach, advancing SLID bonding, based on thin multi-layer stacking of copper and solder was presented enabling highly electromigration-resistant interconnections with pitch less than 30 microns. A first demonstration of this technology was presented along with fabrication, assembly and characterization results. The focus of the next stage of research is suggested below:

- The effect of bonding parameters such as temperature, pressure and time on the rate of formation of Cu_3Sn has to be studied. Based on these results, the SLID bonding assembly process can be optimized for improved manufacturability.
- The ability of this technique to accommodate the die and substrate warpage needs to be studied in detail.
- The bond shear strength needs to be investigated to study the mechanical performance of these intermetallic-based joints.
- Thermal cycling tests are required as a next step to establish the reliability of the copper-solder stacked interconnections at fine pitch and low stand-off height. The role of the CTE mismatch needs to be established using substrate materials such as silicon, glass and organics.
- Electromigration testing is required to verify the higher current-handling capabilities of these interconnections compared to traditional solder-based approaches. The thermal effects of these large currents on the interconnections need to be investigated.

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